Design and Experimental Results of a 2V-Operation Single-Chip GaAs T/R-MMIC Front-End for 1.9-GHz Personal Communications

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Abstract - Design and experimental results of a 2-V operation single-chip GaAs T/R-MMIC front-end are described for 1.9-GHz personal communication terminals. This chip, fabricated with planar self-aligned gate FET process useful for low-cost and high-volume production, integrates RF front-end analog circuits - a power amplifier, a T/R-switch, and a low-noise amplifier. Additionally integrated are a newly designed voltage doubler-negative voltage generator (VDNVG) and a control logic circuit to control transmit and receive functions. The chip is capable of delivering 21-dBm output power at 39% efficiency with 2-V single power supply in transmit mode. By utilizing up-voltage and negative voltages generated from the generator, the new interface circuit enables the switch to handle high power outputs over 24 dBm with 0.55-dB insertion loss.

I. INTRODUCTION

Advanced digital wireless communication terminals such as digital cordless phones and wireless local area network equipment strongly require reduction in the number of RF components as well as RF devices with lower operating voltage, smaller size, and lower cost throughout the world. As reported in some papers, a GaAs Transmit/Receive (T/R)-MMIC front-end is one of the best candidates for these requirements, because GaAs power amplifiers (PAs) and low-noise amplifiers (LNAs) are suitable for achieving high output power, high efficiency, and low-noise figure with low supply voltages than Si ones [1,2].

To realize high-density integration and low single-voltage operation, we have previously developed a single-chip GaAs T/R-MMIC front-end operating with 3-V single voltage operation [3,4]. However, there will be a stronger demand for lower voltage operation of less than 3 V in the near future, because reduction in the number of battery cells is most effective for miniaturizing personal communication equipment [5,6].

This paper describes design and experimental results of a newly developed 2-V operation single-chip GaAs T/R-MMIC front-end for 1.9-GHz personal communications. It delivers 21-dBm output power with 39% efficiency, adjacent channel power leakage (ACP) below -55 dBc, and exhibits high power handling capability of over 24 dBm with only an operating voltage of 2 V in transmit mode.

II. CHIP ARCHITECTURE

Fig. 1 illustrates a chip microphotograph and functional layout of the single-chip GaAs T/R-MMIC front-end. The chip integrates analog RF front-end circuits - a PA, a T/R-switch (SW), and an LNA together with a voltage doubler-negative voltage generator (VDNVG), and a control logic circuit (LOGIC). Thus, both analog and digital circuits are laid out on the chip whose size is 1.35 mm x 2.5 mm. The chip was assembled in a 26-pin surface mount type plastic package for low cost.

In designing FETs, we have employed planar self-aligned

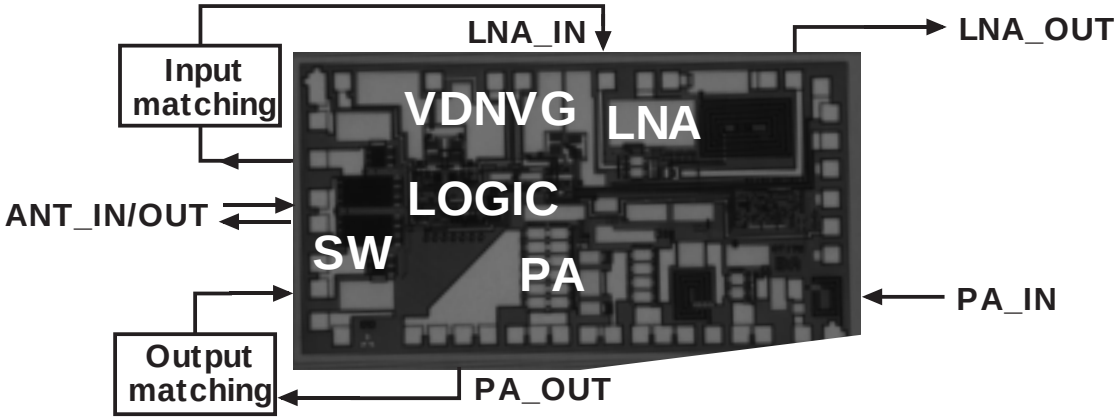

Fig. 1. Chip microphotograph and functional layout for T/R-MMIC front-end.

gate (SAG) power FETs with dual-gate structures, to achieve high gain and low power dissipation operating on 2 V. The newly designed VDNVG produces sufficient negative voltage for biasing a PA and pulls switch bias voltage up higher than supply voltage. The new interface circuit between LOGIC and SW is also incorporated into the chip to enhance switch power handling capability even under a 2-V low power supply condition.

III. FET DESIGN

To realize high-density integration chip with low-cost, high-volume production, we have previously developed three different kinds of planar SAGFETs, including a power FET (Fig. 2(a)) operating on a low voltage of 3 V [3,4].

In addition to these FETs, we have newly developed two different kinds of SAGFETs with dual-gate structures, as shown in Figs. 2(b) and(c). A dual-gate FET usually has higher gain than a single-gate one because of its small gate-source capacitance, thereby enabling a high efficiency operation of the PA even when biased at 2 V. Fig. 2(b) shows the schematic cross-section of the dual-gate power FET. It has a similar structure to cascade connected single-gate power FETs (Fig. 2(a)), due to n^+-layer implanted between the two gates. An offset gate structure is employed for the FET to achieve breakdown voltage of over 8 V. On the other hand, the dual-gate FET for the LNA, as shown in Fig. 2(c), has a symmetric structure with short gate-to-drain space, in comparison with the power FETs (Fig. 2(b)), which leads to high transconductance and RF gain.

Frequency characteristics measured for single- and dual-

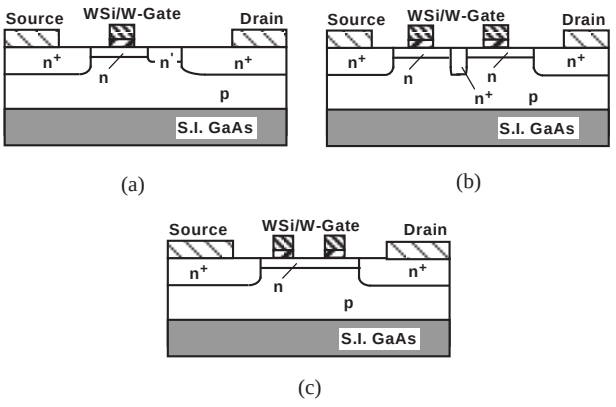

Fig. 2. Cross-sections of (a) single-gate power FET, (b) dual-gate power FET, and (c) dual-gate D-FET for LNA.

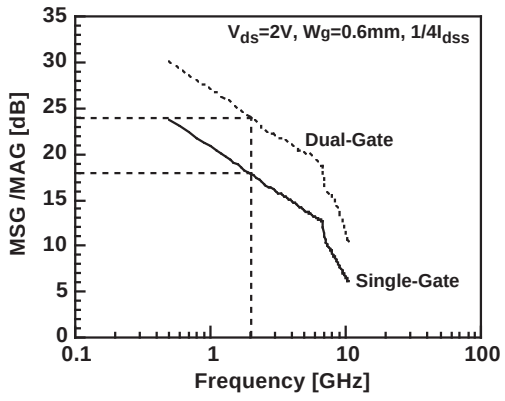

Fig. 3. Small-signal characteristics of single- and dual-gate power FETs.

gate power FETs are shown in Fig. 3. At 2 GHz, the gain of the dual-gate FET is about 6 dB higher gain than that of the single-gate one, which is suitable for realizing high gain and high efficiency operation of the PA.

Thus, in this work, we have used five different kinds of FETs including the previously developed FETs.

IV. Circuit Design And Experimental Results

A. Voltage doubler-negative voltage generator

A GaAs PA usually requires a negative voltage generator (NVG) for its gate biasing [3,4]. There would be, however, the following problems in case that NVGs ever reported are operated on 2 V; (1) a generated negative voltage of -1.2 V is insufficient for biasing a PA which employs power FETs with a -1.8-V threshold voltage, and (2) switch power performance could not handle a power of over 19 dBm even when supplies of both +2 V and -1.2 V are used for switch control [3,4]. Switch power handling capability is often expressed as the following equation:

Power handled: $P=2N^2(V_c-V_p)^2/Z_o$

where N, V_c, V_p, and Z_o denote stacked FET number, control voltage, pinch-off voltage of FET, and system characteristic impedance, respectively [7]. When N = 1, Z_o = 50 ohm, and V_p=2 V, for example, the equation reveals that V_c of at least 3.8 V is necessary for power handling of over 21 dBm.

In order to overcome these problems, therefore, we have designed a new GaAs voltage doubler-negative voltage generator (VDNVG). Fig. 4 shows the schematic circuit of the VDNVG. The VDNVG consists of an oscillator, a voltage doubler, a pole inverter, and a level controller. Since each charge pump circuit consisting of S_1 to S_8 and C_1 to C_4 are complementarily operated, the ripples in the up-voltage, V_{2D}, and a negative voltage, V_N, generated from the doubler and pole inverter are greatly suppressed [3,4]. The level controller converts the voltage, V_N, into the desired gate-bias voltage, V_g. The controller suppresses sufficiently gate-bias voltage deviations even when the PA's gate current flows [3,4]. SPICE simulation was used to optimize the FET widths of drivers in the doubler and pole inverter, in terms of the output voltage difference, V_{delta} (= V_{2D} - V_N), and V_N. Smoothing capacitors, C_2 and C_4, which require large capacitances of over 40 pF in the charge pump circuits, were laid out off-chip to reduce the chip area occupied by the VDNVG.

As shown in Fig. 5, the VDNVG can operate over a very wide supply voltage range from 1.0 V to 6.0 V, and it also produces a V_{2D} of 2.9 V and a V_N of -1.8 V with a current of 5.5 mA under 2-V power supply. Since a V_{delta} of about 4.7 V(=2.9-(-1.8)) is greater than the target voltage of 3.8 V, sufficient switch power performance will be provided, as described later.

Fig. 6 shows the negative voltage characteristics versus supply voltage measured for this work, VDNVG, and the previous one, NVG [3]. The VDNVG can output about 0.6 V lower voltage than the NVG can, by incorporating the voltage doubler into the chip. Measured activation and deactivation times (that is, charge and discharge times) of V_{2D} and V_N were less than 0.5 us and 500 us, respectively. These high-speed

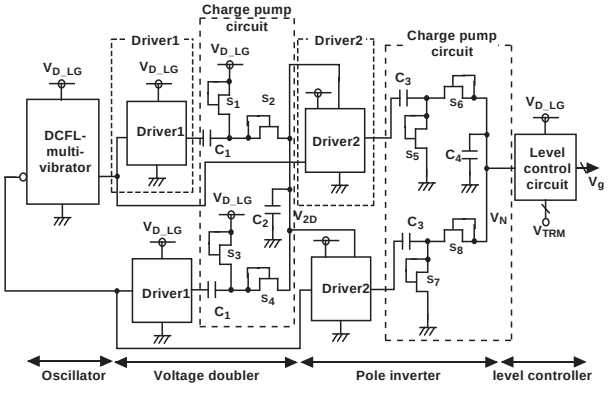

Fig. 4. Schematic circuit for VDNVG.

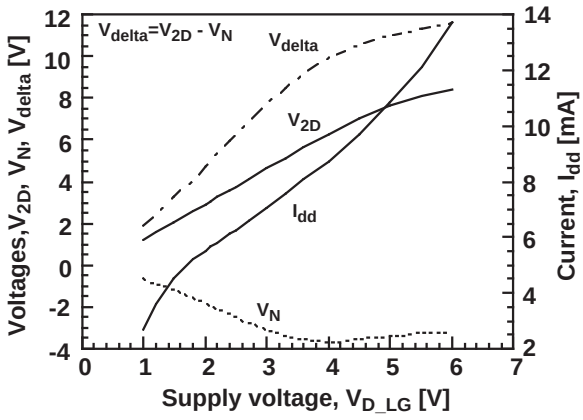

Fig. 5. Supply voltage dependence of VDNVG.

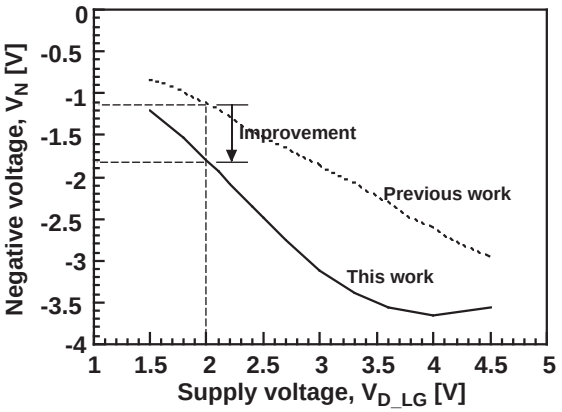

Fig. 6. Measured negative voltage characteritics of VDNVG and previous NVG.

characteristics are most useful for low-current operation in TDMA systems.

B. Power amplifier

Fig. 7 illustrates the schematic circuit of the PA with a three-stage configuration. To obtain high gain and high efficiency under a low voltage condition of 2 V, the dual-gate power FETs are employed for the first-stage. Source- and load-pull measurements were also taken for the final-stage FET in order to investigate optimum impedance operating with both high efficiency and low ACP. All gate-bias voltages are provided through the VDNVG. Input and interstage matching circuits are formed by on-chip lumped elements, bonding wires, and package leads. On the other hand, an output matching circuit is laid out off-chip to reduce chip size and matching loss.

Fig. 8 shows output characteristics of the PA measured under a condition based on the Japanese Personal Handy Phone System (PHS) standard. 21-dBm-output power, 30-dB associated gain, and 39% power added efficiency are obtained for 2-V power supply and ACP of less than -55 dBc. This result indicates that the IC has sufficient output characteristics for the PHS standard. In addition, the gain and efficiency are higher than that of the 2-V operation PA previously reported [5]. We consider that these high gain and efficiency result from optimum design and successful utilization of the dual-gate power FET.

C. Control logic circuit and T/R-switch

As shown in the previous equation, switch power handling capability is dependent on control voltage, V_C. There are some reports on MMIC switches which can handle high output power of 25 dBm or more at a low voltage of 2.0 V or 2.7 V [8,9]. However, these devices require some large spiral inductors, thereby resulting in a quite large chip.

Since the on-chip VDNVG is integrated on the T/R-MMIC chip and a high voltage of about 4.7 V is available to V_C, we have employed a conventional pi-type topology for the SW. This topology offers easily low insertion loss and small occupied chip area.

Fig. 9 shows the schematic for our proposed new interface circuit between the SW and LOGIC. Since the VDNVG oper-

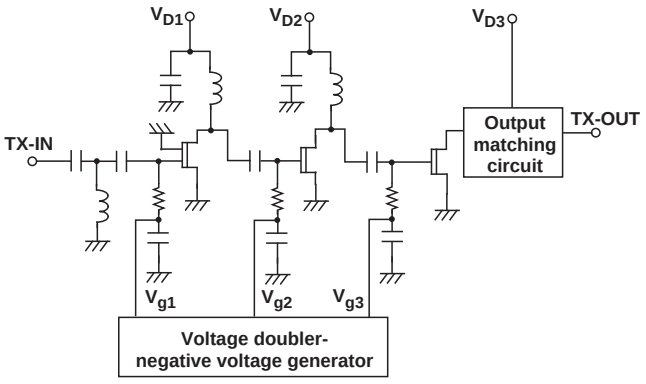

Fig. 7. Schematic circuit for power amplifier biased by VDNVG.

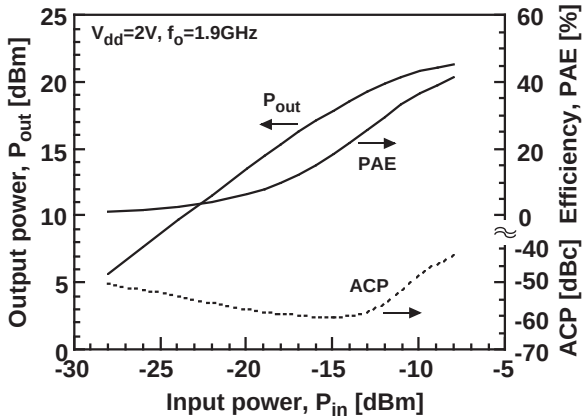

Fig. 8. Output characteritics of power amplifier.

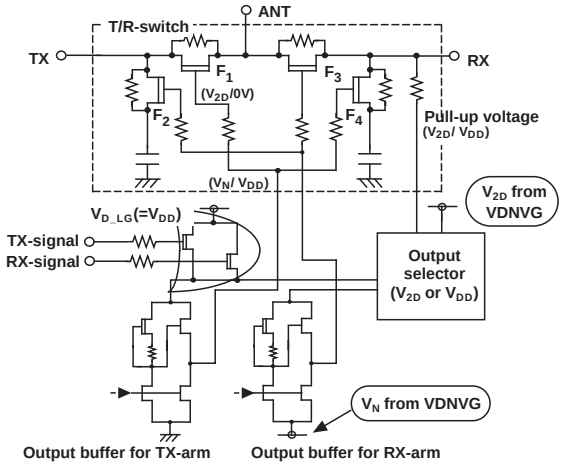

Fig. 9. Schematic interface circuit between SW and LOGIC.

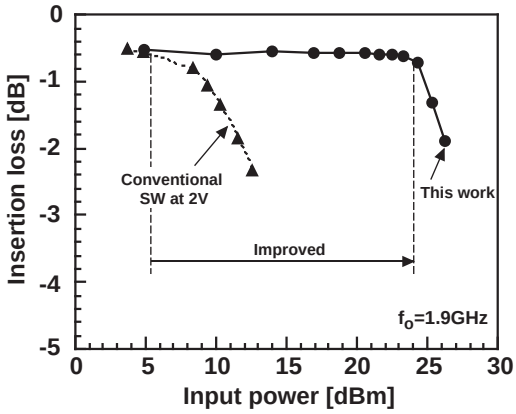

Fig. 10. Transfer characteristics measured in transmit mode.

ates in transmit mode, DCFL output buffers utilizes the voltage difference between the up-voltage, V_{2D}, and the negative voltage, V_N, to enhance the power handling capability. The output selector toggles the pull-up voltage between V_{2D}, and V_{DD}, according to operation mode. DC powers are additionally supplied through an OR gate so that only the part of the circuit necessary for operation of a particular mode can be activated. When the TX- and RX-signals are both 0 V, the LOGIC becomes sleep mode and almost never dissipates current. The resultant current dissipations of the LOGIC for transmit, receive, and sleep modes are as low as 0.20 mA, 0.10 mA, and 0.02 mA.

Fig. 10 shows the transmit-mode transfer characteristics measured for the circuit shown in Fig. 9. As can be seen from the figure, the insertion loss is hardly degraded over the input power range from 5 to 24 dBm. The capability of over 19-dB is improved in comparison with that of the conventional SW operating on 2 V. At 1.9 GHz, the insertion loss is as low as 0.55 dB and the isolation were 30 dB. This result proves that our proposed interface circuit utilizing outputs of the VDNVG can enhance easily switch power performance achieve low-insertion loss even under a 2-V supply condition. The insertion loss and isolation in receive mode were 0.60 dB and 25 dB at 1.9 GHz.

D. Low-noise amplifier

The schematic circuit of the LNA is shown in Fig. 11. The LNA is a self-biased, single-stage amplifier so that it can permit the VDNVG to go to sleep when not transmitting. The dual-gate D-FET shown in Fig. 2(c) is employed for attaining high gain. Only the input matching circuit is fabricated off-chip to reduce chip size and matching loss.

Fig. 12 shows frequency response of the LNA at a drain-bias voltage of 2.0 V. With drain current of 3.5 mA, a gain of 14 dB and noise figure of 1.7 dB are obtained. Utilization of the dual-gate FET gives higher gain and lower current at 2 V, compared to those of the previously reported LNA [3].

Listed in Table I are the main characteristics of the chip. Total current dissipations are as small as 165.7 mA and 3.6 mA in transmit and receive modes.

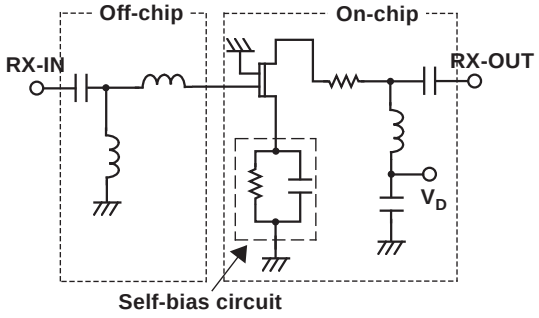

Fig. 11. Schematic circuit for LNA.

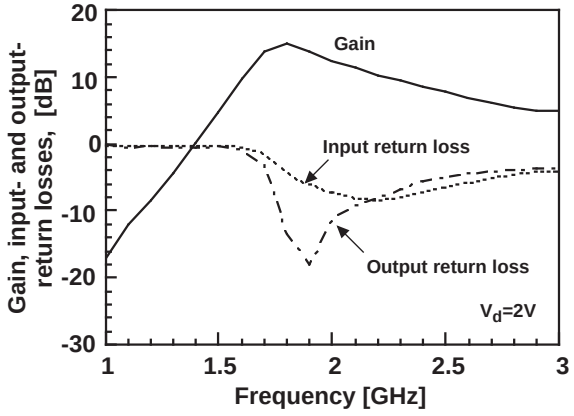

Fig. 12. Measured small-signal characteristics of LNA.

Table I. Main characteristics of T/R-MMIC.

Transmit mode		
PA	Output power	21dBm (ACP < -55dBc)
	Power gain	30.0dB (I_d=160mA, PAE=39%)
SW	Insertion loss	0.55dB
	Isolation	30dB
	Power handled	24dBm
VDNVG	Negative voltage (V_N)	-1.8V (I_d=5.5mA)
	Up-voltage (V_{2D})	2.9V
	Charge time of V_N, V_{2D}	t_{charge}< 0.5µs, $t_{discharge}$< 500µs
Receive mode		
SW	Insertion loss	0.6dB
	Isolation	25.0dB
LNA	Linear gain	14.0dB (I_d=3.5mA)
	Noise figure	1.7dB
Current	Transmit	165.7mA(160mA+5.5mA+0.2mA)
	Receive	3.6mA (3.5mA+0.1mA)
	Sleep	< 0.05mA
Power supply		2.0V single-voltage

V. Conclusion

We have demonstrated design and experimental results of a newly developed 2-V operation single-chip GaAs T/R-MMIC front-end for 1.9-GHz personal communication systems. By incorporating the new FET and circuit technologies into the chip, this IC has excellent performances applicable to PHS terminals. The new FET and circuit technologies presented in this paper will promise both size reductions and low-voltage operation in personal handsets.

Acknowledgement

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