Timing Analysis of an Optically Differential Reconfigurable Gate Array for Dynamically Reconfigurable Processors

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High-speed reconfigurable processors incorporating a reconfigurable memory and microprocessor array into a chip have been developed [1]. Such devices use a context-switching method. Their internal reconfigurable memory includes reconfiguration contexts of 16 banks. One bank includes a reconfiguration context used for ALUs that can be changed to others on a clock in nanoseconds. These devices have achieved rapid calculation capability using quick reconfiguration. Nevertheless, a problem remains: increasing the amount of internal memory is very difficult while maintaining gate density. An Optical Differential Reconfigurable Gate Array (ODRGA) has been developed to realize both rapid reconfiguration capability and high gate density [2]. ODRGA consists of gate-array VLSI, an external optical memory, and laser light sources. This paper presents timing analysis results for reconfiguration and the execution of ODRGA of when it is used for a dynamically reconfigurable processor. This study obtained both experimental results and HSPICE simulation results.

First, the reconfiguration timing was analyzed using a 0.35 μm CMOS process ODRGA-VLSI chip. The reconfiguration time of the ODRGA-VLSI chip is separated into three parts: refresh time, detection time of the optical reconfiguration context, and the response time of differential reconfiguration circuits. The refresh time to fully charge the junction capacitance of photodiodes and the response time of differential reconfiguration circuits were confirmed using HSPICE simulation 1.8 ns and 1.6 ns, respectively. In addition, the photodiode detection time was confirmed by extraction from an experimental result for a period less than 4.4 ns. In that case, the ODRGA-VLSI chip photodiodes were constructed between an N-well and a P-substrate, the size of which was $25.5\mu m \times 25.5\mu m$. A 633 nm - 20 mW He-Ne-Laser was used as a light source for experimentation. As a result, the total reconfiguration time is 7.8 ns because the total time necessary for optical reconfiguration is the sum of those three periods.

A 2bit-Full Adder and 2bit-Multiplier were implemented on an ODRGA-VLSI chip using HSPICE simulation to evaluate the delay time of optically reconfigurable logic blocks, optically reconfigurable switching matrices, and optically reconfigurable I/O blocks in ODRGA-VLSI chip. The Adder and Multiplier delay times were confirmed as 6.5 and 6.6 ns, respectively. Results show that the total period necessary for optical reconfiguration and subsequent execution of the implementation circuit are 14.4 ns at 69 MHz. Nevertheless, the frequency of this dynamically reconfigurable operation can be increased to 128 MHz because the reconfiguration cycle and the execution cycle are separated into individual functions with the same period, as with pipelining of a RISC processor. Moreover, power consumption of the 2bit-Full Adder and 2bit-Multiplier were confirmed to be only 423 mW and 507 mW at 125 MHz, respectively.

In summary, this 0.35 μm CMOS process ODRGA-VLSI chip can be used as a dynamically reconfigurable processor at 128 MHz. ODRGA offers the feature that increasing the gate density never decreases the reconfiguration frequency because the gate array can be reconfigured optically and in parallel. In addition, ODRGA-VLSI chip performance will be improved extremely using advanced process technology.

References

[1] H. Nakano, T. Shindo, T. Kazami, M. Motomura, "Development of dynamically reconfigurable processor LSI," NEC Tech. J. (Japan), vol. 56, no. 4, pp. 99–102, 2003.

[2] M. Watanabe, F. Kobayashi, "An Optically Differential Reconfigurable Gate Array with dynamic reconfiguration circuit," 10th Reconfigurable Architectures Workshop, pp. 188, 2003.