DINESH K. BHATIA — DETAILED RESUME

PERSONAL INFORMATION

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Residence Address	8217 Springvalley Lane Plano, TX 75025 (972) 335-6440
Status	US Citizen, Married, two children

RESEARCH INTERESTS AND SPECIALIZATION

- Biomedical Systems: Low power sensor networks; energy harvesting and energy storage; medical devices; wireless communication; system level design and reliability issues for medical systems.
- Reconfigurable and Adaptive Computing: Architectures, CAD, and Compilation; Heterogeneous System Integration, System level design (SOC); Interconnection estimation and prediction; Architecture and CAD for field-programmable gate arrays (FPGAs); CAD for power aware programmable architectures.
- Theory: Graph theory and its application in VLSI (circuit partitioning, VLSI testing); Fault tolerant architectures.

TEACHING INTERESTS

- Physical design automation of VLSI systems,
- Digital Logic, Switching theory,
- Reconfigurable computing,
- Introduction to Engineering and Contemporary topics in Engineering
- VLSI systems,
- Data structures and algorithms,
- Microsystems design,
- VLSI architecture,
- Combinatorial optimization, Graph theory and algorithms.

Employment History

UTD

- Associate Professor, Department of Electrical Engineering, University of Texas at Dallas, *September 2000-present*.
  Besides teaching, research, and service, also directing an aggressive research group – Embedded and Adaptive Computing Group (www.eac.utdallas.edu)

- Program Head, Computer Engineering Program, Erik Jonsson School of Engineering and Computer Science, University of Texas at Dallas, *October 2004-August 2006.*
  As a program head, lead the development of top rated graduate program. With aggressive recruiting and retention campaign, grew the new program enrollment to about eighty students while maintaining the highest standards (GPA and GRE) in the school. Initiated and implemented doctoral program in computer engineering. Lead the effort with a proposal to initiate BSCE. The undergraduate program approval was obtained from UT System.

UC

- Associate Professor, Department of Electrical and Computer Engineering and Computer Science, University of Cincinnati, *September 97-August 2000.*
- Director, Design Automation Laboratory, University of Cincinnati, *June 91 – August 2000*.
- Assistant Professor, Department of Electrical and Computer Engineering and Computer Science, University of Cincinnati, *June 91 –August 97*.

SMU

- Visiting Assistant Professor, Department of Computer Science and Engineering, Southern Methodist University, September 1990-May 1991.

UTD

- Research/Teaching Assistant, Computer Science Department, University of Texas at Dallas, *January 87 - August 90.*

Other Positions

NTU

- Visiting Researcher, Center for High Performance Embedded Systems, Nanyang Technological University, Singapore, June 2006.

Education

Ph.D.

- Computer Science, University of Texas at Dallas, 1990. *Thesis: Wafer Scale Integration of Mesh Connected Architectures.* (Part of the work was supported by the ACM-SIGDA/IEEE-DATC academic scholarship)

M.S.

- Computer Science, University of Texas at Dallas, 1987.

B.E.

- Electrical Engineering, Regional Engineering College, Suratkal, India, 1985. *Thesis: Speed Control of Brushless DC Motors.*

Awards and Honors

- IEEE Circuits and Systems Society Distinguished Lecturer, 2007-08.
- Honorable Mention for Ph.D. Dissertation Award, EE Department, 2004-2005, Shankar Balachandaran, Advisee.
- Associate Editor, IEEE Transactions on Computers, July 1999-2003.
- Invited Tutorial Speaker, Physical Design of VLSI Systems, IEEE Design and Test Workshop, Delhi, India, August 1999.
- Best MS Thesis Award, ECE Department, 1998-99. Karthik Gajjalapurna, Advisee.
- Embedded Tutorial Speaker, Reconfigurable Computing, IEEE International Conference on VLSI Design, Hyderabad, India, January 1997.
- Tutorial Speaker, Physical Design Automation for Multi-chip Modules, IEEE International Conference on Circuits and Systems, Seattle, June 1995.
- William H. Middendorf Award for Research Excellence, ECECS Department, 1995.
- Commendable Thesis Award, ECECS Department, 1994-95 Giriraj Devaraj, Advisee.
- Best MS Thesis Award, ECE Department, 1993-94. Amit Chowdhary, Advisee.
- Guest Editor, VLSI Design Journal, *special issue on Field-Programmable Gate Arrays,* Gordon Breach Scientific Publishing. 1996.
- Shapiro Visiting Scholar, Dartmouth College, spring 1992. (Honorary assignment for research at Dartmouth)
- ACM - SIGDA/IEEE-DATC Academic Scholarship, June 1990.
- ACM - SIGDA Travel Fellowship, June 1990.
- ACM-SIGDA/IEEE-DATC Special Scholarship, June 1989.
- Who's Who among students in American Universities, 1988-89.
- IIG-CAI Scholarship, Institut of Informatiks, University of Graz, Austria, fall 86.
- Laxman Rao Kirloskar Award for Best EE Student, 1985. (University Rank 1 in Electrical Engineering)

PUBLICATIONS

Journals

1. Sanjay P. Singh, Shilpa Bhoj, Dheera Balasubramanian, Tanvi Nagda, Dinesh Bhatia, Poras Balsara, "Generic Network Interface for Plug and Play NoC based Architecture" International Journal of Electronics, (accepted)
2. A. Hande, T. Polk, W. Walker, Dinesh Bhatia, "Indoor Solar Energy Harvesting for Sensor Network Router Nodes", Journal of Microprocessors and Microsystems-Special Issue on Sensor Systems, (accepted)
3. Abhiman Hande, Todd Polk, William Walker, Dinesh Bhatia, "Self-Powered Wireless Sensor Networks for Remote Patient Monitoring in Hospitals" Sensors 2006, 6, 1102-1117, ISSN 1424-8220.
4. Parivallal Kannan and Dinesh Bhatia, "Interconnect Estimation for FPGAs", IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, Vol. 25, No. 8, pp 1523-1534, August 2006.
5. Shankar Balachandaran and Dinesh Bhatia, "A-priori Wirelength and Interconnect Estimation based on Circuit Characteristics", IEEE Transactions on Computer Aided Design of Integrated Circuits and Systems, Vol 24. No 7 pp 1054-1065, July 2005.
6. Manjunath Gangadhar and Dinesh Bhatia, "FPGA based EBCOT Architecture for JPEG 2000", Journal of Microprocessors and Microsystems, Vol 29, 8-9, pp. 363-373.
7. Shankar Balachandaran, Parivallal Kannan, and Dinesh Bhatia, "On Metrics for Routability Estimation for FPGAs", IEEE Transactions on VLSI Systems, Vol. 12, No. 4, April 2004, pp. 381-385.
8. J. M. Emmert, S. Lodha, and Dinesh Bhatia, "On Using Tabu Search for Design Automation of VLSI Systems, Journal of Heuristics 9(1), pp. 75-90, January 2003, Kluwer Academic Publishers.
9. J. M. Emmert and Dinesh Bhatia, "Reconfiguring FPGA Mapped Design for Fault Tolerant Applications", Journal of Electronic Testing, Volume 16, 591-606, 2000.
10. J.M. Emmert and Dinesh Bhatia, "Two-Dimensional Placement using TABU Search", Journal of VLSI Design, Vol. 12, 13-23, 2001.
11. Dinesh Bhatia and James Haralambides, "Bounds, Designs, and Layouts for Multi-Terminal FPIC Architectures", INTEGRATION – The VLSI Journal, 28 (1999), 141-156.
12. Dinesh Bhatia and James Haralambides "Resource Requirements and Layouts for Field Programmable Interconnection Chips", IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 8. No 3., June 2000
13. Karthik Gajjalapurna and Dinesh Bhatia, "Temporal Partitioning and Scheduling Data Flow Graphs on Reconfigurable Computers", IEEE Transactions on Computers, Vol. 48, No. 6, Pages 579-590.
14. Dinesh Bhatia, "Field Programmable Gate Arrays", Journal of VLSI Design, vol. 4, number 4, 1996.
15. Dinesh Bhatia and V. Shankar, "Greedy Segmented Channel Router", Journal of VLSI Design, Vol. 5, No. 1, Pages 11-21, 1996.
16. Dinesh Bhatia and Amit Chowdhary "A Multi-Terminal Net Router for FPGAs", Journal of VLSI Design, Vol. 4, No. 1, Pages 1-10, January 1996.
17. Dimitrios Kagaris, Spyros Tragoudas, and Dinesh Bhatia, "Pseudo-Exhaustive Built-

In TPG for Sequential Circuits", IEEE Transaction on Computer Aided Design of Integrated Circuits and Systems, Vol. 14, No. 9, Pages 1160-1171, September 1995.

18. R. P. Swaminathan, D. Giriaraj, and D. K. Bhatia. "The pagenumber of the class of bandwidth-k graphs is k – 1", Information Processing Letters, 55(2):71-74, July 1995.
19. Giriraj Devaraj and Dinesh Bhatia, "Crosstalk Driven MCM Router", Journal of Microelectronics Systems Integration, Pages 65–80, Vol. 2, No. 2, 1994.

Journal Submissions and Manuscripts

20. Narayan Subramanian, Rajarshee Bharadwaj, Dinesh Bhatia, "A Power Aware Design Methodology for Leakage Tolerant FPGAs", INTEGRATION – VLSI Journal, December 2006 (submitted)
21. Sanjay P. Singh, Dinesh Bhatia, "Reconfigurable Router Architectures for Rapid NoC Implementations", (manuscript)
22. Rajan Konar, Rajarshee Bhardwaj, Dinesh Bhatia, Poras Balsara, "Exploration of a Power Aware Programmable Architecture", IEEE Transactions on VLSI Systems, (manuscript)
23. Mukesh Chugh, Dinesh Bhatia, Poras Balsara, "Configurable W-CDMA Rake Receiver Architectures", (manuscript)

Book Chapters

24. Dinesh Bhatia, Placement and Routing of Multi-Chip Modules, Chapter 9.2, Pages 643-651, Microsystems Technology for Multimedia Applications: An Introduction, IEEE Press, 1995, ISBN 0-7803-1157-4.

Magazine Articles

25. Dinesh Bhatia, "Field Programmable Gate Arrays", IEEE Potentials, Pages 16–19, February 1994.

Peer Refereed Edited Volumes and Proceedings

26. Dinesh Bhatia, Leonardo Estevez, and Shekar Rao, "Energy Efficient Contextual Sensing for Elderly Care", IEEE Engineering and Medicine and Biology Conference, Lyon, France, 2007 (accepted)
27. Shilpa Bhoj and Dinesh Bhatia, "Pre-Route Interconnect Capacitance and Power Estimation in FPGAs", International Conference on Field Programmable Logic and Applications, Amsterdam, Netherlands, August 2007 (accepted)
28. Shilpa Bhoj and Dinesh Bhatia, "Thermal Modeling and Temperature Driven Placement for FPGAs" IEEE International Conference on Circuits and Systems (ISCAS), New Orleans, May 2007.
29. Rajarshee Bharadwaj, Jathan Rai, Dinesh Bhatia, "Sleep Size: Evaluating Sleeper Cells in Power-gated FPGAs", ACM Symposium on Field Programmable Gate Arrays (FPGA-2007), Monterey, February 2007, (submitted)
30. Narayan Subramanian, Rajarshee Bharadwaj, Dinesh Bhatia, "A Leakage Aware Design Methodology for Power-gated Programmable Architectures", IEEE International Conference on Field Programmable Technology (FPT), Bangkok, Thailand, December 2006.
31. W. Walker, T. Polk, A. Hande, and D. Bhatia, "Remote Blood Pressure Monitoring

Using a Wireless Sensor Network", IEEE Sixth Annual Emerging Information Technology Conference, August 2006.

32. T. Polk, A. Hande, W. Walker, and D. Bhatia, "Wireless Telemetry for Oxygen Saturation Measurements", IEEE Biomedical Circuits and Systems (BiOCAS) Conference, London, UK, November 2006
33. Sanjay P. Singh, Shilpa Bhoj, Dheera Balasubramanian, Tanvi Nagda, Dinesh Bhatia, Poras Balsara, "Generic Network Interface for Plug and Play NoC based Architecture", Lecture Notes in Computer Science, Volume 3985, Reconfigurable Computing: Architectures and Applications, pp. 287-298, 2006. Presented at International Workshop on Applied Reconfigurable Computing (AR2006), Delft, The Netherlands, March 1-3, 2006.
34. Rajan Konar, Rajarshee Bharadwaj, Dinesh Bhatia, Poras Balsara, "Exploring Logic Block Granularity in Leakage Tolerant Programmable Devices", IEEE International Conference on VLSI Design, Hyderabad, pp. 754-757, 3-7 January 2006.
35. Rajarshee Bharadwaj, Rajan Konar, Dinesh Bhatia, Poras Balsara, "FPGA Architecture for Standby Power Management" IEEE International Conference on Field Programmable Technology (FPT), Singapore, pp. 181-188, December 2005.
36. S. Balachandaran, Dinesh Bhatia, "Timing Aware Interconnect Prediction Models for FPGAs", International Conference on Field Programmable Logic (FPL 2005), Tampere, Finland, pp. 167-172, August 2005.
37. Mukesh Chugh, Dinesh Bhatia, Poras Balsara, "Design and Implementation of Configurable W-CDMA Rake Receiver Architectures on FPGA", 12th Reconfigurable Architectures Workshop RAW 2005. Proceedings of the 19th IEEE International Parallel and Distributed Processing Symposium (IPDPS '05) Workshop 3 – Vol 4, p. 145.2, April 04 – 08, 2005.
38. R. Manimegalai, E. Siva Soumya, V. Muralidharan, B. Ravindran, V. Kamakoti, Dinesh Bhatia, "Placement and Routing for 3D-FPGAs using Reinforcement Learning and Support Vector Machines", 18th International Conference on VLSI Design, IEEE Press, January 2005. pp 451 - 456
39. Rajarshee Bhardwaj, Rajan Konar, Poras Balsara, Dinesh Bhatia, "Exploiting Temporal Idleness to Reduce Leakage in Programmable Architectures", 10th Asia and South Pacific Design Automation Conference. Proceedings of the ASP-DAC 2005, Asia and South Pacific Vol 1, 18 – 21 Jan 2005, pp. 651 – 656, Vol 1 .
40. Parivallal Kannan and Dinesh Bhatia, "Estimating Pre-Placement FPGA Interconnection Requirements", Proceedings of the 17th International Conference on VLSI Design, IEEE Press, January 2004. pp 869-874, Jan 05 – 09, 2004.
41. Manjunath Gangadhar and Dinesh Bhatia, "FPGA Based EBCOT Architecture for JPEG 2000", Proceedings of IEEE International Conference on Field Programmable Technology, Tokyo, 15 – 17 December 2003, pp 228 - 233.
42. Parivallal Kannan and Dinesh Bhatia, "Interconnect Estimation for FPGAs under Timing Driven Domains", IEEE International Conference on Computer Design (ICCD), Proceedings of the 21st International Conference on Computer Design, p. 334, October 13 – 15 2003
43. Parivallal Kannan and Dinesh Bhatia, "Interconnection Estimation for Segmented FPGA Architectures", Proceedings of the 16th Annual IEEE International SoC Conference, September 2003, pp 295 – 296 , Sept 17 – 20, 2003 .
44. Shankar Balachandran and Dinesh Bhatia, "A-priori Wirelength and Interconnect

Estimation Based on Circuit Characteristics", ACM International Workshop on System Level Interconnect Prediction, Proceedings of the 2003 International Workshop on System Level Interconnect Prediction, pp 77-84, 2003.

45. Parivallal Kannan, Shankar Balachandaran, Dinesh Bhatia, "Rapid and Reliable Routability Estimation for FPGAs", International workshop on field programmable logic, Montpellier, France, September 2002. Lecture Notes in Computer Science, LNCS 2438, Springer Verlag, Volume 2438, pp. 242-252, ISBN 3-540-44108-5 (2002).
46. Shankar Balachandaran, Parivallal Kannan, and Dinesh Bhatia, "On Metrics for Routability Estimation for FPGAs", IEEE/ACM Design Automation Conference, New Orleans, Proceedings of the 39th Conference on Design Automation, pp. 70-75, June 10 – 14, 2002.
47. Shankar Balachandaran, Parivallal Kannan, and Dinesh Bhatia, "On Routing Demand and Congestion Estimation for FPGAs", Proceedings of joint meeting of 7th Asia and South Pacific Design Automation Conference p.639 and 15th International Conference on VLSI Design, IEEE Press, 07 – 11 January 2002.
48. Parivallal Kannan and Dinesh Bhatia, "Tightly Integrated placement and routing for FPGAs", International workshop on field programmable logic, August 2001. Lecture Notes in Computer Science, LNCS 21476, Springer Verlag, Volume 2147, pp. 233-242, ISBN 3-540-42499-7 (2001).
49. Parivallal Kannan, Shankar Balachandaran, Dinesh Bhatia, "fGREP: Fast Generic Routing Demand Estimation for Placed FPGA Circuits International workshop on field programmable logic, August 2001. Lecture Notes in Computer Science, LNCS 2147, Springer Verlag, Volume 2147, pp. 233-242, ISBN 3-540-42499-7 (2001). Proceedings of the 11th International Conference on Field Programmable Logic & Applications, pp 233 – 242, Aug 27 – 29, 2001.
50. J. M. Emmert and D. K. Bhatia, "Ultra Fast FPGA Placement," International workshop on field programmable logic, September 1999. Lecture Notes in Computer Science, Springer-Verlag, Volume 1673, pp. 81-90, ISBN 3-540-66457-2. (1999).
51. Dinesh Bhatia, Kuldeep Simha, Parivallal Kannan, "NEBULA: A Partially and Dynamically Reconfigurable Computing Environment", International workshop on field programmable logic, September 1999. Lecture Notes in Computer Science, Springer-Verlag, Volume 1673, pp. 81-90, ISBN 3-540-66457-2. (1999).
52. Ravi Kothari, Ming Dong, Dinesh Bhatia, "Neighborhood Induced Stochastic Resonance", International Joint Conference on Neural Networks, 1999. Vol 1, 10 -16 July 1999, pp 621 – 624 Vol 1.
53. J. M. Emmert and D. K. Bhatia, "A Methodology for Fast FPGA Floorplanning," Proceedings of ACM Seventh International Symposium on Field-Programmable Gate Arrays, February 1999.
54. Gregory Tumbush and Dinesh Bhatia, " Clustering to Improve Bi-Partition Quality and Run Time", Proceedings of the 1999 IEEE International Symposium on Circuits and Systems, 30 May – 2 June 1999, pp 145 – 148 Vol 6, January 1999.
55. J. M. Emmert and D. K. Bhatia, "Incremental Routing in FPGAs," Proceedings of 11th Annual IEEE International Application Specific Integrated Circuit Conference, pp 217 – 221, 13 - 16 September 1998.
56. Sandeep Lodha and Dinesh Bhatia, "Bi-partitioning using TABU Search", Proceedings of 11th Annual IEEE International Application Specific Integrated Circuit

Conference, pp. 223 – 227, 13 – 16 September 1998.

57. J. M. Emmert, A. Randhar, and D. K. Bhatia, “Fast Floorplanning for FPGAs,” International workshop on field programmable logic, September 1998. Lecture Notes in Computer Science, Springer-Verlag, Volume 1482, pp. 129-138, September 1998.
58. Dinesh Bhatia, Karthik Gajjalapurna, Kuldeep Simha, Parivallal Kannan, “REACT: Reactive Environment for Runtime Reconfiguration”, International workshop on field programmable logic, September 1998. Lecture Notes in Computer Science, Springer-Verlag, Volume 1482, pp. 209-218, September 1998
59. N. Venkateswaran and Dinesh Bhatia, "Clock-Skew Constrained Placement for Row Based Designs", Proceedings of International Conference on Computer Design (ICCD 98), pp. 219-220, Austin, October 1998.
60. Karthikeya M. Gajjala Purna and Dinesh Bhatia, "Partitioning in Time: A Paradigm for Reconfigurable Computing", Proceedings of International Conference on Computer Design (ICCD 98), pp. 340-347, Austin, October 1998.
61. Karthikeya M. Gajjala Purna and Dinesh Bhatia, "Emulating large designs on Small Reconfigurable Hardware", Proceedings of International Workshop on Rapid Systems Prototyping, Leuven, Belgium, June 3-5, 1998.
62. J. M. Emmert and D. K. Bhatia, “Reconfiguring FPGA Mapped Designs with Applications to Fault Tolerance and Reconfigurable Computing,” International workshop on field programmable logic, September 1997. Lecture Notes in Computer Science, Vol. 1304, pp. 141-150, Springer Verlag, ISBN 3-540-63465-7. (1997).
63. J. M. Emmert and D. K. Bhatia, “Reconfiguring FPGA Mapped Circuits,” CERC/VIUF/IEEE Computer Society Workshop on 21st Century Electronics Systems Design: Breakthroughs in Quality and Productivity, December 1997.
64. Arun Hegde and Dinesh Bhatia, "C to Synthesizable VHDL", CERC/VIUF/IEEE Computer Society Workshop on 21st Century Electronics Systems Design: Breakthroughs in Quality and Productivity, December 1997.
65. K.M. Gajjalapurna and Dinesh Bhatia, "Temporal Partitioning and Scheduling for Reconfigurable Computers", IEEE International Conference on FPGAs in Custom Computing Machines (FCCM 98), pp. 329-330, Napa Valley, April 1998.
66. Raghu Burra and Dinesh Bhatia, "Timing Driven Multi-FPGA Board Partitioning", Proceedings of IEEE International Conference on VLSI Design, Chennai, India, January 1998. Proceedings of the 11th International Conference on VLSI Design: VLSI for Signal Processing, p 234, Jan 04 – 07, 1998.
67. Gregory Tumbush and Dinesh Bhatia, “Partitioning under Area and Timing Constraints”, Proceedings IEEE International Conference on Computer Design (ICCD-97), pp. 614-620, Austin, September 1997.
68. Gregory Tumbush and Dinesh Bhatia, "K-way Partitioning under Timing, Pin, and Area Constraints", Proceeding of IEEE International Conference on Innovative Systems in Silicon (ISIS 97), pp. 95-106, Austin, October 1997.
69. Dinesh Bhatia, “Reconfigurable Computing” Proceedings of Tenth International Conference on VLSI Design, Hyderabad, India, January 04 - 17 1997, pp 356 - 359.
70. Jianzhong Shi and Dinesh Bhatia, “Performance Driven Floorplanning for Field-Programmable Gate Arrays”, ACM International Symposium on Field Programmable Gate Arrays, Monterey, pp. 112-118, February 1997.
71. V. Natesan, Anurag Gupta, Srinivas Katkoori, Dinesh Bhatia, Ranga Vemuri, “A Constructive Method for Data Path Area Estimation During High Level VLSI

Synthesis", Asia and South Pacific Design Automation Conference, (ASP-DAC), pp. 509-515, Chiba, Japan, January 1996.

72. Jianzhong Shi, Dinesh Bhatia, "Macro Block Floorplanning for FPGAs", IEEE Tenth International Conference on VLSI Design, January 1997. IEEE Computer Society Press. Proceedings of the 10th International Conference on VLSI Design, pp 21 – 26, Jan 04 – 07, 1997.
73. Vijayananda Sankar, Dinesh Bhatia, "Multiway Partitioner for High Performance FPGA based Board Architectures", IEEE International Conference on Computer Design (ICCD), Pages 579-585, Austin, October 1996. IEEE Computer Society Press.
74. Doug Smith, Dinesh Bhatia, "RACE: Reconfigurable and Adaptive Computing Environment", International workshop on Field Programmable Logic (FPL), Darmstadt, Germany, September 1996. Lecture Notes in Computer Science, Vol. 1142, pp. 87-95, Springer Verlag, ISBN 3-540-61730-2. (1996).
75. Dinesh Bhatia, James Haralambides, "Bounds for Multi-Terminal Net Routings on FPICs", Proceedings of Canadian workshop on Field-Programmable Logic, Pages 170-177, May 1996.
76. V. Natesan and Dinesh Bhatia, "Performance Driven Placement for Large Synthesized Designs", Proceedings of 1995 IEEE ASIC Conference, Pages 237-240, Austin, September 1995. IEEE Computer Society Press.
77. Dinesh Bhatia, James Haralambides, "Resource Requirements for Field-Programmable Interconnection Chips", Proceedings of Eighth International Conference on VLSI Design, Pages 376-380, New Delhi, India, January 1995. IEEE Computer Society Press.
78. Dinesh Bhatia, Vanitha Narasimhan, "Simple Yet Effective Replication for FPGA Partitioning", Proceedings of IEEE Conference on Application Specific Integrated Circuits, ASIC-94, pp. 152-155, Rochester, September 1994. IEEE Computer Society Press.
79. Harold W. Carter, Dinesh Bhatia, "Automatic Test Vector Generation (ATPG) and Design for Testability for Field Programmable Gate Arrays: A University Perspective", *Invited paper,* PLD Conference, San Jose, April 11–13, 1994.
80. V. Shankar, Dinesh Bhatia, "Generalized Routing for Row-Based FPGAs", Proceedings of Fourth Great Lakes Symposium on VLSI, pp. 64-69, March 1994. IEEE Computer Society Press.
81. Dinesh Bhatia, Amit Chowdhary, Spyros Tragoudas, "Stochastic Model for Routability Analysis of FPGAs", Proceedings of Fourth Great Lakes Symposium on VLSI, pp. 76-79, March 1994. IEEE Computer Society Press.
82. Dinesh Bhatia, Ramesh Rajagopalan, Srinivas Katkoori, "Hierarchical Reconfiguration of VLSI/WSI Arrays", Proceedings of VLSI-94, Calcutta, India, Pages 349-352, January 1994. IEEE Computer Society Press.
83. Amit Chowdhary, Dinesh Bhatia, "Detailed Routing of Multi-Terminal Nets in FPGAs", Proceedings of VLSI-94, Calcutta, India, Pages 237-242, January 1994. IEEE Computer Society Press.
84. Dimitrios Kagaris, Spyros Tragoudas, Dinesh Bhatia, "Pseudoexhaustive BIST for Sequential Circuits", Proceedings of International Conference on Computer Design, ICCD, Pages 523-526, October, 1993. IEEE Computer Society Press.
85. Dinesh Bhatia, "Post Simulation Hardware Prototyping", Proceedings of 1993 SCS

Western Multiconference, Pages 213-218, January 1993, San Diego, CA. Special session on Engineering Education.

86. Dinesh Bhatia, Tom Leighton, Fillia Makedon, Carolyn Norton, "Improved Algorithms for Routing on Two-Dimensional Grids", Proceedings of 18th Workshop on Graph Theoretic Concepts in Computer Science, Wiesbaden, Germany, pp. 114-122, June 1992. Lecture Notes in Computer Science, Vol. 657, pp. 114-122, Springer Verlag, ISBN 3-540-56402-0, ISBN 0-387-56402-0. (1993).
87. Dinesh Bhatia, "Routing with Short Wires and Small Channel Width", Proceedings of 28th Allerton Conference on Communication, Control and Computing, Pages 112-121, Urbana-Champaign, Oct. 1990.
88. Dinesh Bhatia, "Restructuring Wafers for Maximum Yield and some Applications of WSI", Proceedings of 2nd IEEE Symposium on Parallel and Distributed Computing, Pages 750-753, Dallas, Dec. 90. IEEE Computer Society Press.
89. J. David, Dinesh Bhatia, J. Haralambides, Fillia Makedon, "Rip Up and Reroute in a Global Routing Visualization System", EURISCON '91, The European Robotics and Intelligent Systems Conference, Corfu, Greece, June 91.
90. Dinesh Bhatia, Tom Leighton, Fillia Makedon, "Efficient Reconfiguration of WSI Arrays", Proceedings of First International Conference on System Integration, pp. 46-57, Morristown, April 1990, IEEE Computer Society press.
91. Dinesh Bhatia, Fillia Makedon, "A Model for University Computer Learning Resource (CLEAR) Centers " 2nd International Conference on Human-Computer Interaction", Honolulu, Hawaii, August 1987.
92. John Gallant, Dinesh Bhatia, "Statistical Interface between Expert Systems and Databases", New Directions in Database and Knowledge Management Systems, IEEE Computer Society Chapter, Dallas, March 10, 1987.

Poster and Workshop Presentations

93. Shankar Balachandaran, Parivallal Kannan, and Dinesh Bhatia, "Rapid Routability Estimation for FPGAs", ACM Symposium on Field Programmable Gate Arrays, Monterey, February 2002.
94. Parivallal Kannan and Dinesh Bhatia, "Performance and Routability Driven FPGA Placement", Proceedings of VLSI Design and Test Workshops, 2000.
95. *Ultra-Fast Placement for FPGAs,* VLSI Design and Test Workshops, New Delhi, India (August 1999)
96. Lohn M. Emmert, Shankar Balachandaran, Dinesh Bhatia, Layout Algorithms for FPGA, Physical Design Workshops, VLSI Design and Test Workshops, New Delhi, India (August 1999)
97. John M. Emmert and Dinesh Bhatia, "Reconfiguring FPGA Mapped Designs with Applications to Fault Tolerance and Reconfigurable Computing", ACM International Symposium on Field Programmable Gate Arrays, Monterey, February 1997.
98. Akila Subramaniam, Dinesh Bhatia, "Timing Driven Placement with Limited Architectural Interaction for Field Programmable Gate Arrays", First International Symposium on FPGAs, Monterey, February 1995.
99. Dinesh Bhatia, James Haralambides, "On Some Bounds for Field Programmable Interconnection Chips", First International Symposium on FPGAs, Monterey, February, 1995.
100. Dinesh Bhatia, V. S. S. Nair, "Reliable Reconfiguration of WSI Structures",

Fifth SIAM Conference on Parallel Processing for Scientific Computing, March 1990, Houston.

101. Dinesh Bhatia, "Reconfiguring Leveled Networks for Maximizing the Performance", Fifth SIAM Conference on Parallel Processing for Scientific Computing, March 1990, Houston.

Invited Presentations

102. Bucket Based FPGA Architecture for Power Management, Computer Science and Engineering Department, University of Texas at Arlington, April 3, 2007.
103. Wireless Sensor Networks for Biomedical Applications, UT Southwestern Radiological Science and Biomedical Engineering Seminar Series and IEEE Engineering in Medicine and Biology Society Meeting, March 21, 2007.
104. Low Data Rate Wireless Networks Operating on Harvested Energy, Texas Instruments – India, Bangalore, December 2006.
105. Wireless Sensing and Integration for Personal Medical Devices, Distinguished Speaker, International Conference on Medical Electronics, New Delhi, India, December 2006.
106. Research Directions in Reconfigurable and Adaptive Computing, Institute on Infocomm Research (I^2R), Singapore, June 2006.
107. 3D IC Design, VLSI Design Group, CSE Department, Indian Institute of Technology, Chennai, India, December 23, 2005.
108. Advances in Reconfigurable Computing, US Army Vetronics Institute, Winter Workshop Series, January 11, 2005.
109. Reconfigurable Computing, CSE department, Southern Methodist University.(02/04).
110. Reconfigurable Computing for Wideband Signal Processing, US Army Vetronics Institute, Winter Workshop Series, January 14, 2004.
111. Reconfigurable Computing, US Army Vetronics Institute, Winter Workshop Series, December 2-6, 2002.
112. IEEE Dallas Chapter Meeting, Dallas, All about Color on the World Wide Web (September 2001).
113. Computer Aided Design for FPGAs, FPGA Group, Lucent Technologies, Allentown PA, (Spring 97).
114. Design Automation Research at the University of Cincinnati, Physical CAD group, IBM, East Fishkill, NY, (8/96)
115. Physical Package Design for MCMs, Wright Laboratories, Solid State Electronics Directorate. (12/93)
116. Architecture and CAD for Field Programmable Gate Arrays, Advanced FPGA Development Group, Texas Instruments Inc., Dallas, Texas, (9/93).
117. Research Methods in Low-Power Digital Design, Semiconductor Product Design Center, Texas Instruments Inc., Dallas, Texas, (9/93).
118. Field Programmable Gate Arrays, MTL Incorporated, Dayton, Ohio. (9/92)
119. Improved Algorithms for Two Dimensional Grid Routing, Southern Illinois University at Carbondale, Computer Science Department. (11/92)
120. Improved Algorithms for Two Dimensional Grid Routing, Dartmouth College, Mathematics and Computer Science Department. (4/92)

121. Improved Algorithms for Two Dimensional Grid Routing, University of Cincinnati, ECE Department. (4/92)
122. Wafer Scale Integration of Mesh Connected Architectures, University of Cincinnati ECE Dept. (11/90).
123. Reconfiguration and Routing of Wafer Scale Arrays, Southern Methodist University Computer Science and Engg. Dept. (5/90).

PATENTS

1. "METHOD, APPARATUS, AND SYSTEM FOR MANAGING POWER CONSUMPTION OF AN INTEGRATED CIRCUIT", Dinesh Bhatia, Rajarshee Bharadwaj, Rajan Konar, Poras Balsara, Disclosure filed March 2006. Application No. 60/841,455.

FUNDED RESEARCH

Project/Date	Source	Amount
A Software Defined Emergency Radio, 09/06-08/08, Co-Principal Investigator	National Institute of Justice (Department of Justice)	$400,000
Advanced Radars and Electro-optical Sensors (ARES), 2002-2004, Co-Principal Investigator	Defense Advanced Research Projects Agency via Space Missile Defense Command.	$210,000
Congestion and Routability Estimation for Large ASICs, 2002-03, Principal Investigator	ACM/SIGDA	$24,000
High Performance Communication Architectures for SoC Based Network Processors, 2001-02, Principal Investigator	ALCATEL Corporation	$30,000
Algorithms for Physical Design Automation for Field Programmable Gate Arrays, 12/97-06/02, Principal Investigator.	Lucent Technologies.	$63,000
Dynamically Reconfigurable Computing, 6/98-5/00, Principal Investigator.	Ohio Board of Regents	$78,000♣
Highly Reactive Environment for Runtime Reconfiguration, 6/97-6/00,	Defense Advanced Research Projects Agency (DARPA),	$724,761♦

♣ This is joint project with Prof. Jack Jean a Wright State University. His funding is one half of the total amount.

Principal Investigator,	Information Technology Office, BAA 9706.	
Synthesis and Partitioning for Reconfigurable Computers, 7/97-6/99, Co-Principal Investigator.	United States Air Force, Air Force Research Laboratory, BAA 97-07 AAK.	$800,000
Reconfigurable Computing Environment, 7/96-10/99, Principal Investigator.	United States Air Force, Wright Laboratory, BAA 96-01-AAK	$300,822[=]
Dynamically-Reprogrammable Avionics System Technology Implementation Concept (DRASTIC), 7/95-6/97. Principal Investigator.	United States Airforce, WL/AAAT, (SBIR Phase-II sub-contract from MTL). Phase II SBIR AF 94-119.	$153,000
Dynamically-Reprogram able Avionics System Technology Implementation Concept (DRASTIC), 7/94-3/95. Principal Investigator	United States Airforce, WL/AAAT, (SBIR Phase-I sub-contract from MTL). SBIR AF 94-119.	$20,000
Multicomponent Synthesis for Multi chip Modules: Integration of Behavioral, Test and Package Compilation Techniques, 1/94-9/96. Investigator.	United States Air-Force, Wright Laboratories, Solid State Electronics Directorate.	$77,000
Reconfigurable (Hardware) Computing, 6/96-5/97, Principal Investigator.	University Research Council, University of Cincinnati.	$4,976
Rapid Prototyping Solutions for Digital Designs, 3/93-9/93, Principal Investigator.	MTL Systems Inc., Dayton.	$5,400
Architecture and CAD tools for Rapid Prototyping, 1/92-12/92. Principal Investigator.	University Research Council, University of Cincinnati.	$5,000

In addition to the funded research, a whole range of CAD tools software, equipment for rapid prototyping, and hardware has been acquired through industrial contributions.

♦ The three year funding from DARPA is going to be $699,761. Remaining $25,000 are real matching funds for equipment.

[=] The three year funded amount from Air Force is $221,822. The remaining $79,000 are real matching funds (with no overhead) in support of students and equipment.

SUPERVISED RESEARCH

Ph.D Students

1. Todd Polk, "Self-Powered Wireless Sensor Networks for Telemedicine Applications", expected to graduate in Summer 2007.
2. Shilpa Bhoj, "Power and Thermal Aware 3D FPGA Architectures", expected to graduate in Spring 2008.
3. Shailendra S. Aulakh, "Core based Reconfigurable Architectures", Started September 2001.
4. Fredrick Rush, "Routing Algorithms for High Density Designs", Started January 2001.
5. Rajarshee Bhardwaj, "Architecture and Design Methodology for Power Gated Programmable Fabrics", graduated Fall 2006, Texas Instruments.
6. Shankar Balachandaran, "A-Priority Interconnect Estimation for Field Programmable Gate Arrays", Graduated Summer 2005, Assistant Professor, Indian Institute of Technology at Madras, Chennai, India.
7. Parivallal Kannan, "Interconnection Estimation and Routability Prediction for FPGAs", Graduated December 2003, Employed with Xilinx.
8. John Martin Emmert, "Algorithms for Physical Mapping of Circuits to Field Programmable Gate Arrays", May 1999, Associate Professor, University of North Carolina at Charlotte.
9. Gregory Tumbush, "Partitioning under Multiple Constraints", Graduated March 1998, Air Force Research Laboratory, WPAFB, Ohio.
10. Venkateswara Natesan, "A Framework for Estimation and Synthesis of VLSI Layouts". Graduated November 1996, Employed with IBM at East Fishkill, NY.

M.S. Thesis Students*

11. Praveen Aroul, "Cardiac Pacemaker Architecture", started September 2006.
12. Kumarswamy Ramanathan, "Low Power Architectures for Video Processing", started September 2006. (jointly advised with Prof. Poras Balsara)
13. William Preston Walker, "Energy Scavenging from Natural Resources for Sensor Network Processing" Jonsson School GetDoC recipient, started January 2005.
14. Joel Votaw, "Asynchronous Microcontrollers for Ultra Low Power Sensor Architectures", started January 2005.
15. Sanjay P. Singh, "Modeling and Analysis of Router Architectures and Network Interface Architecture for Network on Chip", graduated October 2006. Texas Instruments.
16. Tanvi Nagda, "Memory Architectures for NoC based Socs", graduated Fall 2006,

* Only those students that work on MS research and publicly defend a MS thesis are listed.

M.S. Emerging Memory Technologies.

17. Jathan Rai, “Design of Power Aware Buckets for Programmable Architectures”, Fall 2006, AMD.
18. Narayan Subramanian, “Floorplanning for Power Aware FPGA Architectures”, graduated December 2005. Texas Instruments.
19. Rashida Rajagara, “Routing Architectures for VPGAs”, graduated Spring 2005. Qualcomm.
20. Rajan Konar, “Exploration of Power Aware Programmable Architectures”, graduated February 2005. Freescale Semiconductors.
21. Mukesh Chugh, “Design and Implementation of Configurable W-CDMA Rake Receiver Architectures on FPGA”, graduated December 2004, Mathworks.
22. Manjunath Gangadhar, “Hardware based Acceleration for JPEG 2000”, graduated December 2003. Intel Corporation
23. Hem Neema, “Comparative Study of Algorithms implemented in Software and FPGA based Hardware”, Graduated February 2001. Xilinx Corporation.
24. Chakrapani Gollamudi, “Evolutionary Design of Digital and Analog Circuits”, Graduated February 2001. Hewlett Packard.
25. Vikas Sharma, “FPGA Floorplanning”, Graduated September 2001.
26. Deepak Mekaraj, “A Flexible Framework for Optimized Temporal Partitioning”, January 2001, Intel Corporation.
27. Pranav Rastogi, “Object oriented design methods for reconfigurable computing”, December 2000, Intel Corporation.
28. Sandeep Lodha, “Partitioning for FPGA Based Architectures”, Graduated September 1999. Synopsys Inc.
29. Sunil Alexandar, “Graph Algorithms on Reconfigurable Architectures”, October 1999, CADENCE.
30. Mandeep Singh, “A Framework for Testing and Validation of Adaptive Computing Systems”, expected completion May 1999, SUN Microsystems.
31. Karthik Gajjalapurna, “Temporal Partitioning and Scheduling for Reconfigurable Computers”, September 1998, Synopsys Inc. Best Thesis Award, 1998-99.
32. Kuldeep Simha, “NEBULA: A Partially and Dynamically Reconfigurable Architecture”, September 1998, Hewlett Packard.
33. Arun Hegde, “C to Synthesizable VHDL”, January 1998, Digital Equipment Corporation (DEC).
34. Akash Randhar, “Macro Block Based FPGA Floorplanning”, December 1997, Texas Instruments.
35. Raghu Burra, “Timing Driven Partitioning for Board Level Architectures”, October 1997, Lucent Technologies.

36. Doug Smith, “Reconfigurable and Adaptive Computing Environment”, June 1997, SUN Microsystems.
37. Vijayanand Sankar, “Board Level Partitioning for Programmable Architectures”, Graduated, October 1996, Intel Corporation.
38. Jianzhong Shi, “FPGA Floorplanning”, September 1996, Lucent Technologies.
39. Rajasekhar Medicherla, “Routing in Multi-Segmented FPGA Architectures”, Graduated May 1996, employed with VIEWlogic Systems Inc.
40. Ramesh Rajagopalan, “Delay Optimization for Multi-FPGA Partitioning”, Graduated December 1994, employed with SUN Microsystems Computer Corporation.
41. Akila Subramaniam, “Timing Driven FPGA Placement”, Graduated, September 1994, employed with Synopsys Inc.
42. Giriraj Devaraj, “Placement and Routing for Multi-chip Modules”, Graduated March 1994. Employed with Mentor Graphics Corporation. Commendable Thesis Award 1994-95.
43. Vanitha Narasimhan, “Replication Based Partitioning for FPGAs”, Graduated March 1994, employed with VIEWlogic Systems Inc.
44. Venkatraman Shankar, “Routing in Row Based Field-Programmable Gate Arrays”, Graduated Dec. 1993, employed with Intel Corporation.
45. Amit Chowdhary, “Routability Analysis and Routing in Logic Cell Arrays”, Graduated August 1993, Best Thesis Award 1993-94.

Undergraduate Projects

46. Uday Gurnani, “Wireless Body Temperature Monitoring”, Fall 2006.
47. Aidan Skoyles, “Hardware Based Data Encryption” Senior project and honor’s thesis. *Eugene McDermott Scholar at UTD*.
48. Deborah Edwards, “Speech Recognition Hardware” 2003.
49. John Miller, “Reconfigurable Computing Systems”, 2001-2002.
50. Lydia Porzucek, “Image Processing”, 2000-2001.
51. Brad Beckman, Kevin Lake, Joe Potkay,”Hardware Implementation of Adobe Photoshop Filters”, 1999-2000.
52. Paul Campisi, “A GUI Based FPGA Floorplanner”, 1995-96.
53. Patrick Allen, “CAD Tool for Generating Layouts of Field-Programmable Interconnection Chips”, 1995-96.
54. Todd Broch and Kevin Broch, “Hardware for Configurable Computing”, 1994-95.
55. Eric Jubin and George Moussa, “Design of Application for Configurable Computer”, 1994-95.
56. Peter Hodakievic, “Repairing Ultra Large Random Access Memory”, 1993-94.

57. Robert Cheek, “Cost Driven Heterogenous K-way Partitioning”, 1993-94.
58. Heather Howard, “SNOOPY: Monitor for PCI Bus”, 1993-94.
59. Jeff Walrath and Chris Kiszely, “Maze Routing Chip”, 1992-93.
60. Jeffery Scott and Thomas Green, “ECE: Elegant Compression Engine”, 1992-93.
61. Mark Stevens, “General Purpose Prototyping Board”, 1992-93.
62. Basem Nayfeh and David Berman, “Image Compression Architecture for Animated Video”, 1991-92.
63. James Carter, “Electronic Billboard Graphics Engine Integrated Circuitry”, 1991-92.
64. Tom martin and Dean Arriens, “Hand-held Master Mind Game”, 1991-92.
65. Kevin Rolfes, “Music Synthesis under MIDI Control”, 1991-92.
66. Dave Lauerhauss and Eric Jones, “Hand-held Dungeons and Dragons Game”, 1991-92.

Other Projects

1. Steve Foland, “Wireless Sensor Networking” CLARK Foundation Scholar, The University of Texas at Dallas, Summer 2005.

SERVICE RELATED ACTIVITIES

University of Texas at Dallas 2000-

1. Member, Best Doctoral Dissertation Award Committee, EE Department, 2006-07.
2. Member, Faculty Senate, The University of Texas at Dallas, 2006-07.
3. University Library Committee 2005-2006.
4. Program Head, Computer Engineering, January 2004-August 2006.
5. Vice Chair, University Information Resources Security, Planning, and Policy Committee, 2005-2006.
6. Chair, University Library Committee, 2004-05.
7. Chair, Faculty Search Committee, Computer Engineering (Search 767), 2004-05.
8. Member, Executive Committee of Industrial Advisory Board on Research, Erik Jonsson School of Engineering and Computer Science, December 2004-
9. Member, Faculty Search Committee, Electrical Engineering Department, 2004-05.
10. Chair, Computer Engineering Program Governance Committee, January 2004-
11. Member, Faculty Search Committee, Computer Engineering Program, 2003-04.
12. Member, Faculty Search Committee, Electrical Engineering Department, 2003-04.
13. Chair, Computing Resources Committee, EE Department, September 2002-present.
14. Chair, Computer Engineering Graduate Program Committee, January 2001-2004.
15. Member, Power Outage Committee, Erik Jonsson School of ECS, 2002-2003.
16. Member, Faculty Senate, The University of Texas at Dallas, 2002-2003.
17. Chair, Electrical Engineering Faculty Search Committee, 2002-2003.

18. Reappointment Review Committees, 2001-2002.
19. Electrical Engineering Faculty Search Committee, 2001-2002.
20. Computing Resources Committee, EE Department, January 2001- August 2002.

University of Cincinnati 1991-2000

1. Graduate program coordinator, Computer Engineering, ECECS Department, (June 1999-2000).
2. Faculty Search Committee, ECECS Department, 1997-98.
3. OBR Distinguished Professor search committee, 1997-98.
4. University Research Council Awards Committee, Physical Sciences and Engineering, 1996.
5. Computing resources manager, ECECS Department, 1996-2000.
6. Doctoral examination coordinator, Computer Systems Design Program, ECECS Department, 1994-1996.
7. Undergraduate computer engineering curriculum committee, ECE department, (June 1991-2000).
8. Graduate computer engineering curriculum committee, ECE department, (June 1991-2000).
9. Ph. D. examination committee, 1991-2000.
10. Advise hardware and software upgrades in the microsystems design laboratory.
11. Space and Equipment Committee, ECE–CS Merger, 1993-94.

Academic and Research Service

1. Technical Program Chair, 2007 IEEE Dallas Engineering in Medicine and Biology Workshop, Dallas, November 2007.
2. Publicity Chair, Sixth IEEE Dallas Circuit and Systems Workshop, Dallas, November 2007.
3. Panelist, National Science Foundation, 2007.
4. Program Committee, IEEE International Conference on Field Programmable Technology, Kitakyushu, Japan, December 2007.
5. Program Committee, 17th International Conference on Field Programmable Logic, Amsterdam, Holland, August 2007.
6. Activities Chair and Member of Executive Committee, IEEE Dallas Chapter, 2007.
7. Program Committee, IEEE 2nd International Workshop on Reconfigurable Computing Education, Porto Allegre, Brasil, May 2007.
8. Publicity Chair, Fifth IEEE Dallas Circuit and Systems Workshop, Dallas, October 29-30 2006.
9. Program Committee, Fourteenth International Conference on Advanced Computing & Communications (ADCOM 2006), Suratkal, India, December 2006.
10. Program Committee, IEEE International Conference on Field Programmable Technology, Bangkok, Thailand, December 2006.
11. Panelist, National Science Foundation, 2005.
12. Program Committee, 16th International Conference on Field Programmable Logic, Madrid, Spain, August 2006.
13. Program Committee, IEEE Computer Society Workshop on Reconfigurable Computing Education, Karlsruhe, Germany, March 2006.
14. Program Committee, 15th International Conference on Field Programmable Logic, Tempere, Finland, September 2005.

15. Program Committee, IEEE International Conference on Field Programmable Technology, Brisbane, Australia, December 2004.
16. Associate Editor, IEEE Transactions on Computers, 1999-2003.
17. Program Committee, International Conference on Field Programmable Logic, Antwerp, Belgium, September 2004.
18. Program Committee, International Conference on Field Programmable Logic, Lisbon, Portugal, September 2003.
19. Program Committee, IEEE International Conference on VLSI Design, New Delhi, India, January 2003.
20. Session Chair, Dynamic Reconfiguration Session, International Conference on Field Programmable Logic, Montpellier, France, September 2002.
21. Program Committee, International Conference on Field Programmable Logic, Montpellier, France, September 2002.
22. Program Committee, Joint meeting of 7th Asia and South Pacific Design Automation Conference and 15th International Conference on VLSI Design, Bangalore, India, January 2002.
23. Program Committee, IEEE International Conference on VLSI Design, Bangalore, India, January 2001.
24. Program Committee, PACT'99 Workshop on Reconfigurable Computing (WoRC'99), Newport Beach, CA, October 1999.
25. Guest Editor, Special Issue on Field-Programmable Gate Arrays, VLSI DESIGN Journal, Gordon Breach Science Publishers.
26. Tutorial Speaker, "Reconfigurable (Hardware) Computing", IEEE International Conference on VLSI Design, Hyderabad, India, January 1997.
27. Program Committee, ED-MEDIA 96, World Conference on Educational Multimedia and Hypermedia, Boston, June 1996.
28. Tutorial Speaker, "Physical Design for Multi-Chip Modules", IEEE International Symposium on Circuits and Systems, Seattle, June 1995.
29. Session Chair, VLSI Routing Session, Fourth Great Lakes Symposium on VLSI DESIGN, Notre Dame, March 1994, IEEE.

Reviewer

1. ACM Transactions on Design Automation of Electronic Systems (TODAES) 2003.
2. International Conference on Field Programmable Logic, 2003.
3. ACM/IEEE Design Automation Conference, 2003.
4. International Conference on Field Programmable Logic, 2002.
5. IEEE Transactions on CAD of VLSI Systems, 1999-
6. IEEE Transactions on Computers, 1998-
7. IEEE Transactions on VLSI Systems, 1994.
8. Information Processing Letters 1994.
9. SIAM Journal of Discrete Mathematics 1993.
10. INTEGRATION - the VLSI Journal 1993.
11. International Journal on VLSI Design 1994-present.
12. International Journal of Computer Aided VLSI Design,
13. Journal of Computer System Sciences 1990-91.
14. Tenth International Conference on VLSI DESIGN (IEEE Sponsored),
15. Ninth International Conference on VLSI DESIGN (IEEE Sponsored),

16. Eighth International Conference on VLSI DESIGN (IEEE Sponsored),
17. Seventh International Conference on VLSI DESIGN (IEEE Sponsored),
18. Fourth Great Lakes Symposium on VLSI DESIGN (IEEE and ACM Sponsored),
19. International Conference on System Integration (IEEE sponsored),
20. Second Annual Symposium on Parallel and Distributed Computing (IEEE sponsored),
21. 11th International Conference on Distributed Computing Systems (IEEE sponsored).

Proposal Reviewer

1. National Science Foundation
2. State Board of Education of Idaho
3. State of Maryland

PROFESSIONAL AFFILIATIONS

1. Senior Member, Institute of Electrical and Electronics Engineers (IEEE),
2. IEEE computer society,
3. IEEE Circuits and Systems Society,
4. IEEE Engineering in Medicine and Biology Society,
5. Eta-Kappa-Nu.