ECE165 – Digital Integrated Circuit Design

2006-2007 Catalog Description: VLSI Digital Systems. Circuit characterization, performance estimation, and optimization. Circuits for alternative logic styles and clocking schemes. Subsystems include ALUs, memory, processor arrays, and PLAs. Techniques for gate arrays, standard cell and custom design. Design and simulation using CAD tools.

Prerequisites: ECE 108 grade C- or better.

Text Books: 1) Jan Rabaey, "Digital Integrated Circuits: A Design Perspective", Prentice Hall (Required).
2) Weste & Eshraghian, "Principles of CMOS VLSI Design", Addison Wesley (Reference).

Course Objectives: To teach the engineering and design principles of VLSI (Very Large Scale Integration) CMOS technology for application in digital integrated circuits and subsystems.

Course Topics:

1. VLSI CMOS technology and device fabrication overview. Review of MOSFET transistor device, static and dynamic behavior via analysis and SPICE circuit models and simulations. Review of the CMOS inverter. Designing Combinational Logic Gates, with Layout Design Rules and CMOS Layout Techniques. Scaling and submicron technology issues.
2. Alternative Logic Styles, Static and Dynamic. Low Power CMOS Design.
3. Sequential Logic Circuits. Bistability, Flip-flop classification. Static Sequential Circuits, Dynamic Sequential Circuits. Pipeline Logic Styles.
4. Designing Arithmetic Building Blocks. Logic circuits for Adders, Multipliers, Shifters, and Datapath design in Digital Processor Architectures. Power Considerations in Datapath structures.
5. Coping with Interconnect. Capacitive, Resistive, and Inductive Parasitics. Comments on Packaging Technology.
6. Timing Issues in Digital Circuits. Clock Skew and Sequential Circuit Performance. Alternative Clocking Styles. Self-Timed Circuit Design. Synchronous versus Asynchronous Design.
7. Designing Memory and Array Structures. Memory classification and Memory Core design. Peripheral Memory Circuits. Memory Reliability and Yield.
8. Design Methodologies. Custom versus Cell versus gate array design. FPGA (Field Programmable Gate Array) and related technologies. Design Synthesis and Validation and Testing of Manufactured Circuits.

Class/laboratory schedule: 3 hours lecture, 1 hour discussion, 4 hours labs per week.

Evaluation Methods: Graded by homework/lab assignments, Midterm Exam and Final Exam.

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Contribution of course to meeting the professional component: College level mathematics (probability, ordinary differential equations), engineering topics (digital integrated circuits) , design (group projects and homework)

Relationship of Course to Program Outcomes

1. *An understanding of the underlying principles of, and an ability to apply knowledge of mathematics, science and engineering to electrical engineering problems:*
   Emphasis: 2 Assessment: 1
   An overview of CMOS integrated circuit fabrication technology is followed by a review of fundamental semiconductor science in terms of devices and models for digital integrated circuits. Then the design principles for combinational and sequential circuits are studied to implement boolean digital logic functions. The circuits are mathematically analyzed for their performance and characterization. CAD tools, primarily Cadence Design Systems supports Spice and VHDL simulations at the circuit, layout, switching, logic, and behavioral levels. Basic combinational subsystems, such as arithmetic components, and basic sequential subsystems, such as memory arrays and PLAs for finite state machines, are studied. These building blocks are designed, simulated and characterized for incorporation into electronic engineering applications. *Assessment:* homework/laboratory design and computer simulation problem sets. Midterm and Final Exams are problem based.

2. *An ability to design and conduct experiments, as well as to analyze and interpret data:*
   Emphasis: 0 Assessment: 0

3. *A knowledge of electrical engineering safety issues:*
   Emphasis: 0 Assessment: 0

4. *An ability to design a system, component, or process to meet desired needs:*
   Emphasis: 2 Assessment: 1
   The design of VLSI CMOS integrated circuits components and subsystems is the primary emphasis. These components are characterized to meet desired performance by mathematical analysis and computer simulations of the integrated circuit designs. Typically a logic function is specified, designed with a logic circuit style, simulated using Cadence Spice simulations. Additionally, the circuit layout is completed with Cadence and extraction to SPICE for circuit simulation/verification is possible. Finally, Verilog simulations are incorporated to allow for behavioral simulation of a boolean function as well as a structural logic simulation/verification. *Assessment:* Homework/Project design and simulation exercises.

5. *a) An ability to collaborate effectively with others, b) an ability to function on multidisciplinary teams:*
   Emphasis: 5a): 1 5b): 0 Assessment: 5a): 1 5b): 0
   Projects are performed by design teams of 3 students. This is to simulate real world design team collaborative efforts. *Assessment:* Project grading.

6. *An ability to identify, formulate, and solve engineering problems:*
   Emphasis: 1 Assessment: 1
   Supplementing design issues, discussion and lectures address real world design and manufacturing topics, such as timing, voltage scaling, power consumption, interconnects, testability and device fabrication yields. *Assessment:* Homework and exam problems where these engineering factors are considered.

7. *An ability to use the techniques, skills, and modern engineering tools necessary for engineering practice, including familiarity with computer programming and information technology:*
   Emphasis: 2 Assessment: 1
   Extensive use of Computer Aided-Design (CAD) tools are used in the design, simulation and performance characterization of the integrated circuits and subsystems. *Assessment:* Homework/Laboratory design problems.

8. *An understanding of professional and ethical responsibility:*
   Emphasis: 0 Assessment: 0

9. *An ability to communicate effectively a) in writing, b) verbally, c) with visual means:*
   Emphasis: 9a): 1 9b): 0 9c): 1 Assessment: 9a): 1 9b): 0 9c): 1
   Laboratory reports with circuit simulation plots. *Assessment:* Homework and exam problems include questions asking for explanation of results.

10. *The broad education necessary to understand the impact of engineering solutions in a global and societal context:*
    Emphasis: 0 Assessment: 0

11. *A recognition of the need for, and the ability to engage in, life-long learning:*
    Emphasis: 1 Assessment: 0
    Instruction stresses that only the fundamentals of VLSI CMOS design are covered and that many topics are not covered. The instruction lays a foundation on which later more specialty learning can be supplemented. Advanced texts and research papers are also given.

12. *A knowledge of contemporary issues:*
    Emphasis: 1 Assessment: 0