Silicon-on-Insulator Technology

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Abstract - This article explains the issues related to silicon-on-insulator technology. As the bulk silicon CMOS processes are reaching there limit in terms of device miniaturization and fabrication, SOI technology gives a good alternative to that. SOI technology is considered to take the CMOS processing to its ultimate scalability, and a brief review of work published by many research groups is presented in this paper. Firstly, technological development on fabrication of silicon–on-insulator wafers is presented. After that focusing upon CMOS technology, different types of SOI MOSFETs and related physical concepts are evaluated. Finally double gate MOSFET's properties, and its pros and cons over bulk CMOS technology are explained.

I. Introduction

CMOS integrated circuits are almost exclusively fabricated on bulk silicon substrates for two obvious reasons: the abundant supply of silicon wafers, and because the good oxide can be readily grown on silicon, which is not possible on germanium or on some other semiconductors. The primary motivation for scaling CMOS devices is the increased functionality per cost and the improved performance of devices. As the scaling continues it becomes harder to fabricate devices without compromising performance due to undesirable effects such as threshold voltage roll-off, drain induced barrier lowering (DIBL) and degraded subthreshold slope. These effects cause device to device variations, increase the off current, and decrease the on current. Beside the short channel effects a number of technological barriers exist. As the gate length is reduced the wavelength of the light for the lithography equipment needs to reduce. Manufacturing such optical equipment at smaller wavelength becomes harder due to the availability of materials that should be used for these wavelengths. As gate length is reduced, gate oxide thickness must also be reduced, resulting in an increase in quantum mechanical tunneling in excessively high electric fields. Eventually silicon oxide must be replaced with a high-k material so the physical thickness of the material can be increased. As the device length is reduced the high doping is required in between the source and drain which in turns increases the parasitic capacitance between diffused source, drain and substrate. The doping profile of the devices needs to be controlled more accurately with each new generation, and the implantation and annealing technology needs to keep up with the stringent requirements of very sharp doping profiles. Considering all these facts for a long time search for the breakthrough technology has been undergoing.

Silicon-on-insulator (SOI) technology gives many advantages over bulk silicon CMOS processing. In particular higher speed, lower power dissipation, high radiation tolerance, lower parasitic capacitance, low short channel effects, high subthreshold voltage swing, manufacturing compatibility with the existing bulk silicon CMOS technology. In this paper some of the SOI COMS models which are currently considered as an alternative to bulk CMOS technology and related concepts are presented.

II. Fabrication of SOI wafers [ref. 1,2]

Many techniques have been developed for producing a film of single-crystal silicon on top of insulator. Some of them are based on the epitaxial growth of silicon on either a silicon wafer covered with an insulator (homo-epitaxial techniques) or on a crystalline insulator (hetro-epitaxial techniques). Other techniques are based on recrystallization of thin silicon layer from the melt (laser recrystallization, e-beam recrystallization and zone-melting recrystallization). Silicon-on-insulator can also be

produced from a bulk silicon wafer by isolating a thin silicon layer from the substrate through the formation and oxidation of porous silicon (FIPOS) or through the ion beam synthesis of a buried insulator layer(SIMOX, SIMNI and SIMON). Finally, SOI material can be obtained by thinning a silicon wafer boned to an insulator and mechanical substrate (wafer bonding BESOI). Every approach has its advantages and its pitfall, and the type of application to which the SOI materials is destined, dictates the material to be used in each particular case. **SIMOX** and **UNIBOND** are seems to be the ideal candidates for VLSI CMOS application, while wafer bonding is more adapted to bipolar and power applications. Now we'll review some of the techniques have been used in producing the SOI materials.

a. Hetro-epitaxial Techniques: Hetro-epitaxial Silicon-on-insulator films are obtained by epitaxially growing a silicon layer on a single-crystal insulator (see figure 1). The films are grown using silane or dichlorosilane at temperatures around 1000^0C. All the insulating substrates have thermal coefficients which are 2-3 times higher than that of silicon which generated lot of stresses at interface. Therefore, thermal mismatch is the single most important factor determining the physical and electrical properties of silicon films grown on bulk insulators. *Silicon-on-sapphire (SOS)* is one of single most mature of all hetro-epitaxial materials used. SOS is fabricated by epitaxial growth of a Si film on Al_2O_3. The electrical properties may suffer from lateral stress, in-depth inhomogeneity of the film, and defective transition layer at the interface. Good quality 100 nm thick films, on 6 in. SOS wafers are now available.

b. Homo-epitaxial techniques: *Epitaxial lateral overgrowth,* method consists of growing a single-crystal Si film, from the substrate (i.e. the seed) through and above the SiO_2 layer. ELO process requires a post-epitaxy thinning of the Si film, which can for example be achieved by using a patterned oxide, the silicon film in excess is removed leaving an isolated Si island (dotted line) in the BOX. The main application of ELO technique is the integration of 3-D stacked circuits.

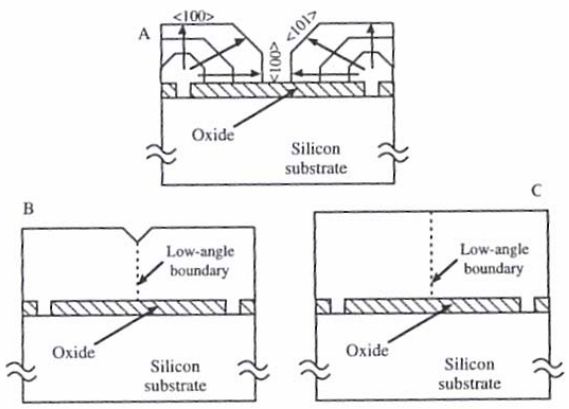

Fig-1: ELO technique. A) growth from seeding window, B) coalescence of adjacent crystals, C) self-planarization of the surface.

c. Recrystallization Techniques: MOS transistor can be fabricated on large grained polysilicon deposited on oxidized silicon substrate. But the presence of grain boundaries brings about low surface mobility and high thershould voltages. Mobility and thershould voltages values can be improved by passivating the dandling silicon bond via hydrogen plasma treatment. High performance ICs however require much better device properties, and grain boundaries must be eliminated from the deposited silicon film. This is the goal of all recrystallization techniques such as Laser beam, E-Beam, zone melt recrystallization. Laser and e-beam both are relatively slow processes (uses a pointed energy source) compared to zone melting method in which incoherent light or near IR source is used.

d. FIPOS: In *Full isolation by oxidized porous silicon* anodic reaction is used to convert a particular region (predefined by p-type doping) of the Si wafer into porous silicon. During subsequent oxidation, the porous Si transforms very rapidly and selectively in a BOX. FIPOS may be able, in the future, to combine SOI circuits with electroluminescent porous Si devices.

e. SIMOX: In the last decade, the dominant SOI technology was SIMOX, which is synthesized by

internal oxidation during the deep implantation of oxygen ions into a Si wafer. Annealing at high temperature restores the crystalline quality of the film. SIMOX 8 in. wafers have good thickness uniformity, low defect density (except threading dislocations: 10^4–10^6 cm^{-2}), sharp Si–SiO_2 interface, robust BOX, and high carrier mobility. Some basic processes of SIMOX are described in figure 2 and figure 3.

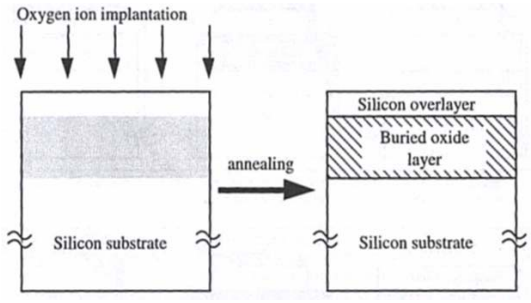

Fig-2: The principal of SIMOX: a heavy dose oxygen implantation into silicon followed by an annealing step produces a buried layer of silicon dioxide below a thin single crystal silicon overlayer.

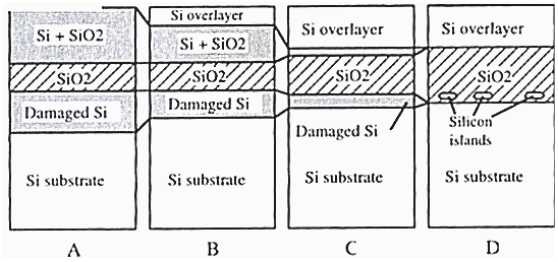

Fig-3: Evolution of the structure of the SIMOX structure as a function of post-annealing temperature (implant dose= 1.5 10^{18} cm^{-2}, energy = 200 keV). A) as implanted, B)2-hr. annealing at 1150^0C , C) 6 hour annealing at 1185^0C, D) 6 Hr. annealing at 1300^0.

f. ***Wafer bonding (WB):*** Wafer bonding and etch back is another mature SOI technology. An oxidized Si wafer is mated to a second Si wafer. When two flat, hydrophilic surfaces such as oxidized surfaces are placed against one another, bonding naturally occurs, even at room temperature, which forms the hydrogen bonds across the gap between two surfaces. After bonding, upper wafer is thinned down from 600microns to few microns to reach the target thickness of the silicon film. The thinning is usually done grinding followed by chemical-polishing or grinding followed by etch-back process (preferred). In etch-back process a P^+ layer is formed at the surface near the oxide where the etching is required and using proper etchant the bare Si surface above the bonded SiO_2 is obtained with approximately 12nm surface tolerance.

g. **UNIBOND:** This material again belongs to the family of wafer bonding structures. But unlike the wafer bonding method, in UNIBOND, the etch-back process is avoided. The revolutionary Smart-Cut mechanism uses the deep implantation of hydrogen (dotted line in figure 4) to generate microcavities. After bonding and annealing, the wafers separate naturally at a depth defined by the location of hydrogen microcavities which have eventually coalesced. The UNIBOND wafer is finished by touch polishing. The smart-cut approach has several outstanding advantages:

I. no etch-back step, with much better uniformity of surface (0.15nm)

II. the prime-quality wafer A is fully recyclable and UNIBOND reduces to a single wafer process, only conventional equipment is needed for mass production, relatively inexpensive 12 in. wafers are manufacturable, and

III. unlimited combinations of BOX and film thicknesses can be achieved in order to match most device configurations (ultra-thin CMOS or thick-film power transistors and sensors).

The defect density in the film is very low, the electrical properties are excellent, and the BOX quality is comparable with that of the original thermal oxide. It is worth noting that the two interfaces of the BOX are ideally organized: the top interface (film–BOX) has the high quality expected from thermal oxidation whereas the bonded interface, of poorer quality, is located underneath the BOX and has little influence on the SOI device performance. A fascinating aspect is that the smart-cut process is adaptable to a variety of materials: SiC or III–V compounds on insulator, silicon on diamond or glass, etc. The

possibility to enroll, in the SOI-based microelectronics, these materials with large band gap, photonic, or high-temperature capabilities opens exciting prospects for the integration of totally new types of devices.

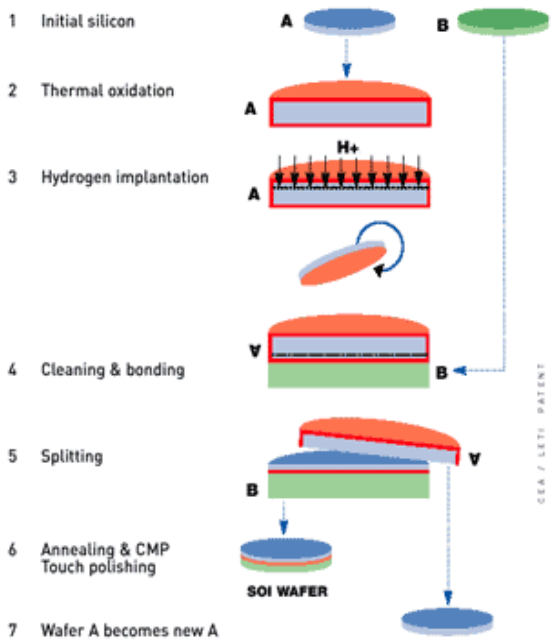

Fig- 4: UNIBOND Process flow, created by 'Michel BRUEL' from LETI [ref-3]

III. Silicon-0n-Insulator MOSFETs

SOI MOSFETs can be categorized into ***fully depleted*** and ***partially depleted*** **MOSFETs** based upon the depletion layer state. In partially depleted state, silicon film thickness is larger than sum of the width of depletion regions from back and front ends. So there is no interaction between these regions, and there exists a piece of neutral silicon beneath the front depletion region. If this neutral piece of silicon, called “body”, is connected to ground by a “body contact”, the characteristics of the device is exactly same as the bulk device. But if this body is left electrically floating, the device will basically behave as a bulk device, but with the notable exception of two parasitic effects, the first one is ***kink effect or floating body effect***, and second on is the presence of parasitic open based NPN bipolar transistor between source and drain. Kink effect is basically appearance of a kink in the output characteristics of an SOI MOSFET. It is generally observed for the floating (unconnected) p-well and presence is because of under high drain to source voltage the electron at drain end create the electron-hole pairs, due to impact ionization mechanism, and are collected in floating body, i.e. p-well and increase the threshold voltage. Also inset the FD and Pd figures. Fig: Showing the kink effect.

On the other hand if the thickness of the silicon film is small and depletion region from both sides meet at the threshold voltage, then the device is called fully depleted. Fully depleted devices are virtually free of kink effect, if their back-interface in not in accumulation region.

The first SOI transistors, dates back to 1964, were partially depleted devices fabricated on silicon-on-sapphire (SOS) substrates. SOS technology was successfully used for numerous military and civilian applications and is still being used to realize commercial HF circuits in fully depleted CMOS. Once the first SOI substrates (the insulator is now silicon dioxide) were available for experimental MOS device fabrication, partially depleted technology the natural choice derived from SOS experience. Partially depleted CMOS continues to be used nowadays and several commercial IC manufacturers have SOI products and product lines such as microprocessors and memory chips. Variations on the partially depleted SOI MOSFET theme include devices where the gate is connected to the floating body. These devices, which have been called "voltage-controlled bipolar-MOS device", "hybrid bipolar-MOS device", "gate-controlled lateral BJT", "multiple-threshold CMOS", "dynamic threshold MOS", or "variable-threshold MOS" have ideal subthreshold characteristics, reduced body effect, improved current drive, and superior HF characteristics. They are mostly used for very low-voltage (0.5 V) applications.

The first fully depleted SOI MOSFET date back to the early 1980's where it was quickly established that these devices exhibited superior transconductance, current drive and subthreshold

swing. In addition to the "regular", inversion-mode devices it was shown that accumulation-mode FD SOI MOSFETs can be fabricated. These possess characteristics comparable to those of inversion-mode devices. The first publication describing a double-gate SOI MOSFET dates back to 1984 [8]. This initial paper predicted the good short-channel characteristics of such a device. The first fabricated double-gate SOI MOSFET was the "fully DEpleted Lean-channel TrAnsistor (DELTA, 1989)", where the silicon film stands vertical on its side (figure 7) [9]. Later implementations of vertical-channel, double-gate SOI MOSFETs include the FinFET [10], the MFXMOS, the triangular-wire SOI MOSFET (figure 9) [11] and the Δ-channel SOI MOSFET (figure 9)[12]. Volume inversion was discovered in 1987[4], and the superior transconductance brought about by this phenomenon were first experimentally observed in 1990 in the first practical implementation of a planar double-gate MOSFET called the "gate-all-around" (GAA) device [13] (figure 8).

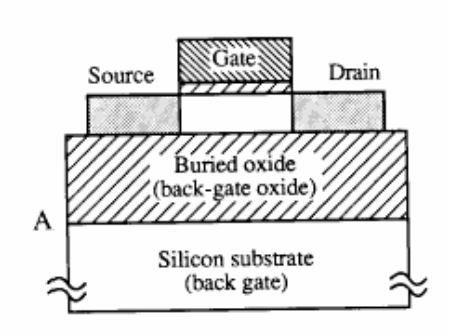

Fig- 5: Conventional thin film SOI MOSFET

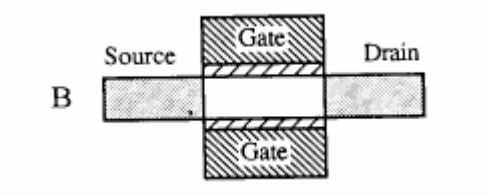

Fig- 6: SOI MOSFET with top and bottom gate

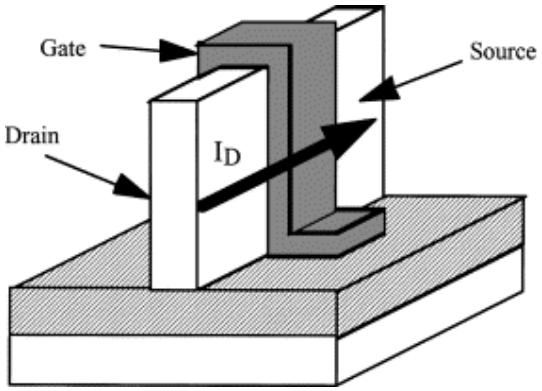

Fig- 7: DELTA/FinFET structure

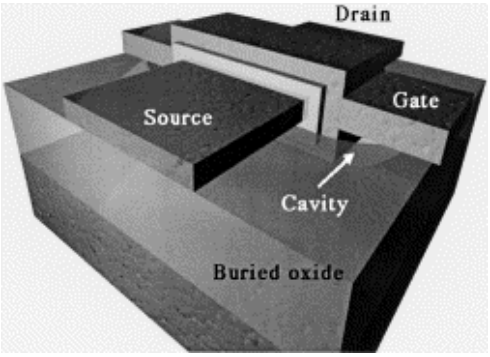

Fig- 8: Gate-all-around (GAA) MOSFET

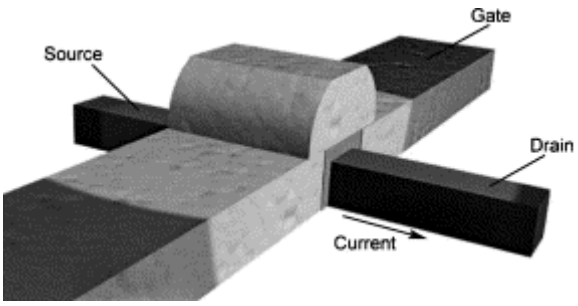

Fig- 9: Triple-gate SOI MOSFET.

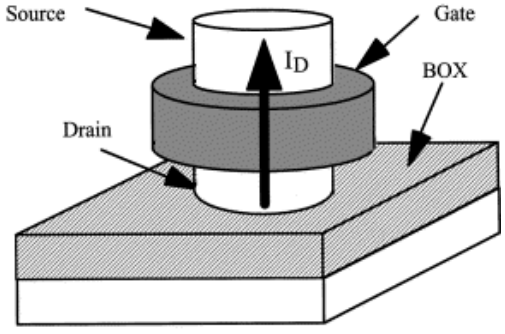

Fig- 10: CYNTHIA/surrounding-gate MOSFET structure.

IV.Double-gate metal–oxide–semiconductor

Double-gate metal–oxide–semiconductor field-effect-transistors **(DGMOSFETs)** are currently considered a serious alternative to standard-bulk MOSFETs to increase the integration capacity of silicon technology in the near future. A dual-gate-silicon-on-insulator DGSOI Structure consists, basically, of a silicon slab sandwiched between two oxide layers (Figure 6). A metal or a polysilicon film contacts each oxide. Each one of these films acts as a gate electrode front and back gate, which can generate an inversion region near the Si–SiO2 interfaces, if an appropriate bias is applied. Thus we would have two MOSFETs sharing the substrate, source, and drain. In the following sections some of the important concepts are presented.

The salient features of the DG FET [23] (Figure 11) are control of short-channel effects by device geometry, as compared to bulk FET, where the short-channel effects are controlled by doping (channel doping and/or halo doping); and 2) a thin silicon channel leading to tight coupling of the gate potential with the channel potential.

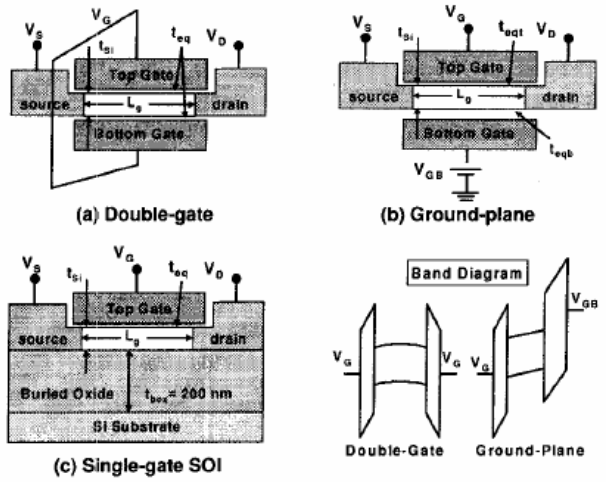

Fig- 11: Double gate, (b) ground plate, (c) single-gated SOI MOSFET. Gate work function is set at mid-gap of the silicon film band gap. On chip biasing of the ground plate is assumed. The source/drain junction is abrupt. The channel length is the metallurgical channel length.

These features provide potential DG FET advantages that include 1) reduced 2D short-channel effects leading to a shorter allowable channel length compared to bulk FET; 2) a sharper subthreshold slope (60 mV/dec compared to >80 mV/dec for bulk FET) which allows for a larger gate overdrive for the same power supply and the same off-current; and 3) better carrier transport as the channel doping is reduced (in principle, the channel can be undoped). Reduction of channel doping also relieves a key scaling limitation due to the drain-to-body band-to-band tunneling leakage current. A further potential advantage is more current drive (or gate capacitance) per device area; however, this density improvement depends critically on the specific fabrication methods employed and is not intrinsic to the device structure.

The most common mode of operation of the DG FET is to switch the two gates simultaneously. Another use of the two gates is to switch only one gate and apply a bias to the second gate to dynamically alter the threshold voltage of the FET [24]. In this mode of operation, called “ground plane” (GP) or back-gate (BG), the subthreshold slope is determined by the ratio of the switching gate capacitance and the series combination of the channel capacitance and the non-switching gate capacitance, and is generally worse than the DG FET. A thin gate dielectric at the non-switching gate reduces the voltage required to adjust the threshold voltage and preserves the drain-field-shielding advantage of the double-gate device structure. However, a thinner gate dielectric also means extra capacitance that does not contribute to channel charge for switching. Since the back-gate FET is very similar to a single-gated SOI FET with an adjustable threshold voltage [24].

DGMOSFETs are claimed to be more immune to short channel effects (**SCE)** than bulk silicon MOSFETs and even more than single gate fully depleted SOI MOSFETs. This is due to the fact that the two gate electrodes jointly control the carriers, thus screening the drain field from the channel. This latter feature would permit a much greater scaling down of these devices than ever imagined in conventional MOSFETs.

a. Short channel effects: Figure 12 and 13 show the threshold voltage roll-off and drain

voltage barrier lowering of double gate for with t_{eq} = 1.5 and 1.0 nm with t_{si} from 5-25 nm. The V_T is determined at V_{DS} = 0.05 V, the DIBL is defined as V_T (V_{DS}=0.05) - V_T (VDS = 1.0), the transconductance is measured at V_{DS} = 1.0 V, V_G = V_T (V_{DS}=0.05) + 0.5 V, and the output conductance is measured at the same V_G, and V_{DS} = 0.75 V

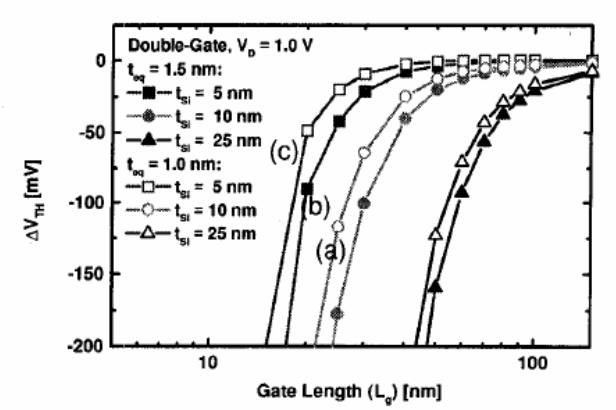

Fig-12: Threshold voltage roll-off for double gate with t_{eq} = 1.5 and 1.0 nm.

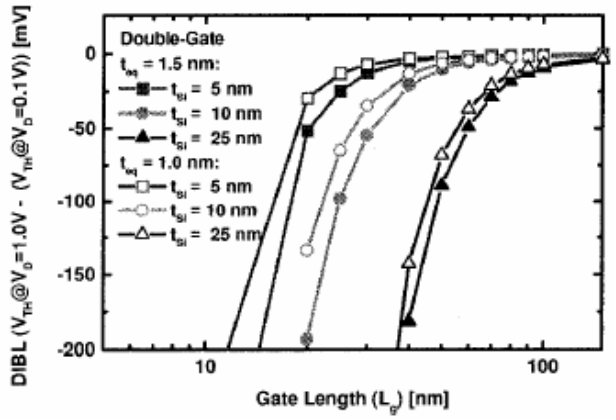

Fig-13: DIBL for double gate with t_{eq} = 1.5 and 1.0 nm.

The threshold voltage roll-off becomes much better as the t_{si} is reduced to 5 nm from 25 nm. Figure 14 compares the V_{th} roll-off for double gate and a single gate SOI. This also reflects the better performance of DG MOSFET in terms of SCE as threshold voltage roll-off is significantly lower for DG MOSFET as compared to SG MOSFET. Single gated ultra thin SOI with an undoped channel does not have the required short-channel control even for the ultra-thin t_{si}(~1.5 nm). Doping the ultra-thin channel uniformly does not improve short channel behavior and only serves to shift the V_{th}.

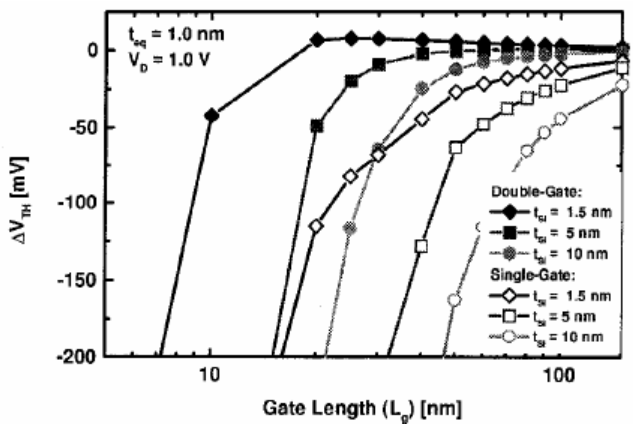

Fig-14: Threshold voltage roll-off for double gate and single gate MOSFET. Single gate will not meet the short channel effect requirements.

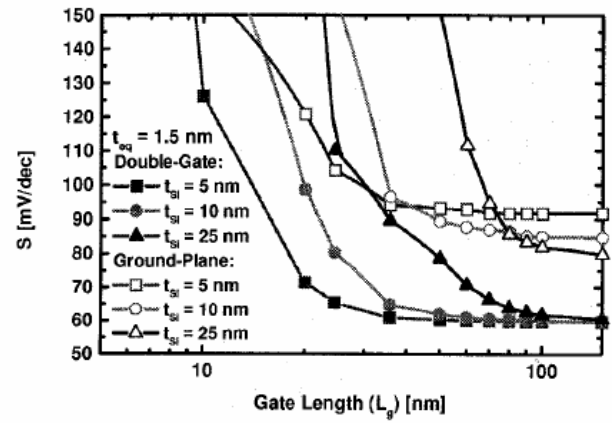

Fig-15: The S-factor for DG MOSFET and for ground plate MOSFET. For DGMOSFET very close to ideal is achievable and for ground plate DIBL is 20-30 mV/dec worse than the double gate. The fixed bottom gate potential results in a capacitor divider, reducing the control of top channel potential by the top gate. Bottom gate insulator for ground plate is 2.25nm thick.

b. SOI/Self Heating: SOI devices also exhibit self heating effects. These arise in SOI devices because the device is thermally insulated from the substrate by the buried oxide layer. This leads to a substantial elevation of temperature within the SOI device, which consequently modifies the output characteristics of the device. The self-heating becomes more pronounced as device dimensions are reduced into the submicron regime because of increased electric field density

and reduced silicon volume available for heat removal. These effects must be taken into account by device technology engineers and designers.

c. Quantum mechanical effects: Modern day transistors experience quantum mechanical effects due to the confinement caused by the band bending near the surface. For an SOI device besides the potential well produced by the bend banding the silicon channel is already confined physically due the thickness of the silicon channel. Due to the ultra thin nature of the silicon channels used for the DG FETs quantization effects will be seen. Ouisse [14] solved the Poisson's and Schrodinger's equations self-consistently in ultra-thin silicon-on-insulator structures, and has studied the interaction between the front and back inversion layers as a function of the silicon film thickness, electron concentration (see figures 17 and 18), and temperature [14]. Based on his study the quantization of energy of the carriers will influence the fundamental electrical characteristics in two ways: (1) Distribution of carriers (2) Mobility of carriers [7, 17]. More details analysis of these two factors can be found later in this paper.

d. Concept of volume inversion: The outstanding feature of these structures lies in the concept of volume inversion, introduced by Balestra *et al* [5]; if the Si film is thicker than the sum of the depletion regions induced by the two gates, no interaction is produced between the two inversion layers, and the operation of this device is similar to the operation of two conventional MOSFETs connected in parallel. However, if the Si thickness is reduced, the whole silicon film is depleted and an important interaction appears between the two potential wells. In such conditions the inversion layer is formed not only at the top and bottom of the silicon slab i.e., near the two silicon–oxide interfaces, but throughout the entire silicon film thickness. It is then said that the device operates in ''**volume inversion**,'' i.e., carriers are no longer confined at one interface, but distributed throughout the entire silicon volume.

Several authors have claimed that volume inversion presents a significant number of advantages, such as

i. enhancement of the number of minority carriers

ii. increase in carrier mobility and velocity due to reduced influence of scattering associated with oxide and interface charges and surface roughness

iii. as a consequence of the latter, an increase in drain current and transconductance

iv. decrease of low frequency noise

v. a great reduction in hot-carrier effects

e. Misalignment of top and bottom gate: The complexity of the DG fabrication, in particular the fabrication and of the bottom gate and it's alignment with the top gate, is still a serious limitation for the industrial development of planar DG technology. Although there exists technologies to fabricate double-gate like structures self aligned (such as in a FinFET or All Around Gate structures) it is not clear which approach will be used to fabricate DGFETs since most proposed methods have not been tried in a manufacturing environment yet. In the case of a fabrication methodology used that can not guarantee that the back and front gates can not gave perfect alignment there will be degradation in the performance of the device [15]. If the effect of this misalignment is known, then a design strategy that can minimize performance degradation can be used. Figure 10 shows the cases studied to simulate the effects of misalignment [15]. Two design cases were considered (see figure 16), (1) Oversized bottom gate to guarantee back-channel control by the bottom gate (2) Minimum bottom gate to minimize the overlap capacitance to source and drain. For oversized gate design, as the gate overlap tolerance $L_o v$ is increased the delay degraded rapidly. Also for a given amount of shift the minimum bottom gate design delay degrades faster than oversized back gate configuration due

to loss of current drive on top of the increased capacitance. It was concluded that the gate alignment tolerance needs to be less than 1/4 of the gate length for suppressing short channel effects. Also the variation in the thickness of the channel needs to be less than 15%. This requirement will become harder to achieve as the silicon thicknesses are scaled down to few atomic layers. Self-alignment in double gate structures is very critical; otherwise device performance decreases rapidly due to overlap capacitance and/or loss in current drive.

Because of these problems and to avoid this limitation the Hisamoto et al. introduced the delta [5] and finfets structures with lateral gates [22].

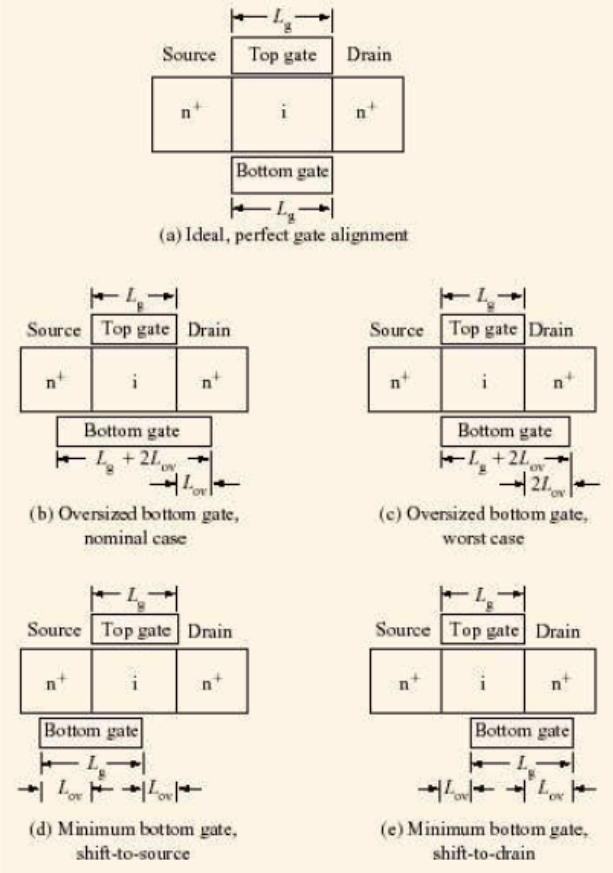

Fig- 16: Cases of misalignment in DGMOSFETs

f. Electron distribution and mobility dependence upon thickness:

f1. Gamiz et al. [7] have studied the electron distribution and mobility behavior in double-gate silicon-on-insulator (undoped silicon layer) silicon inversion layers, and compared it to the mobility in single-gate silicon-on-insulator devices. Electron quantization in the inversion layer was appropriately taken into account, self-consistently solving Poisson's and Schrodinger's equations (see figures 17 and 18) [14]. The effects of phonon scattering, surface roughness scattering, and finally, Coulomb scattering were taken into account. The role played by each scattering mechanism was analyzed as a function of silicon slab thickness and transverse effective field.

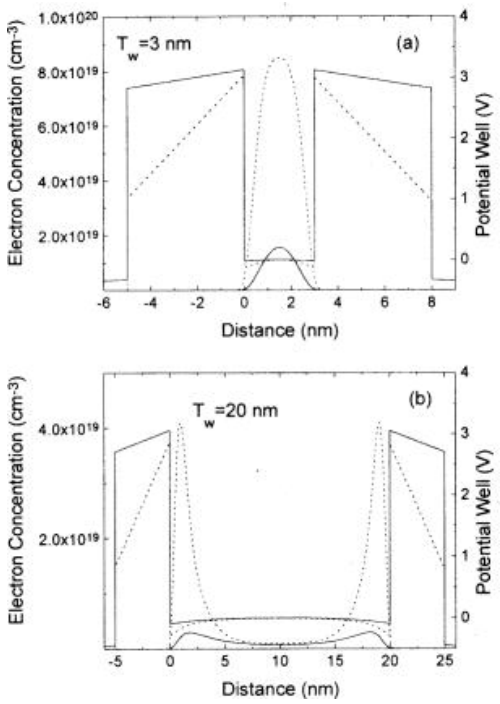

Fig-17: Electron distributions for different thicknesses of the silicon slab in a DGSOI structure. Two different effective electric field values were considered [7]

The research demonstrates that the contributions of surface scattering mechanisms are by no means insignificant. The electron mobility in DGSOI devices as *Tw* decreases was compared with the mobility in SGSOI structures, a. when only phonon scattering was considered, b. when the effect of surface roughness scattering was taken into account in addition to phonon scattering and finally, c. when the contribution of Coulomb interaction with the charges trapped at the interfaces was also taken into consideration

(in addition to phonon and surface roughness). Figure 19 shows the electron mobility as determines by Gamiz et al.

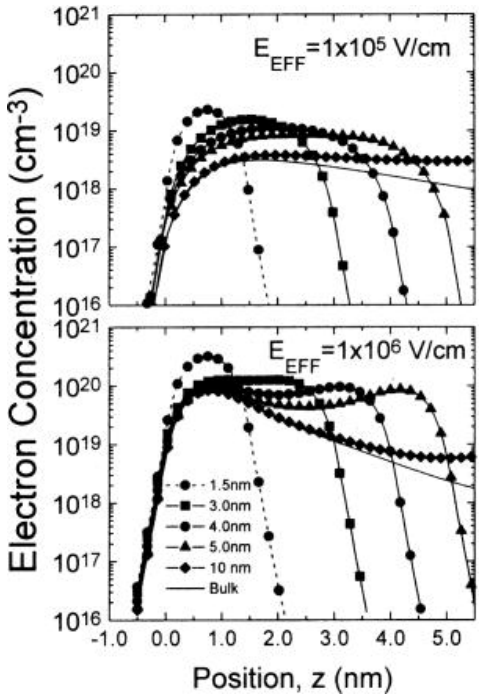

Fig-18: Potential well and electron distribution in a DGSOI inversion layer for two different inversion charge concentrations (solid line: N_{inv} = 1.3×10^{12} cm^{-2} and dashed line: N_{inv} = 8.5×10^{12} cm^{-2}). The oxide thickness was assumed to be 5 nm. [7]

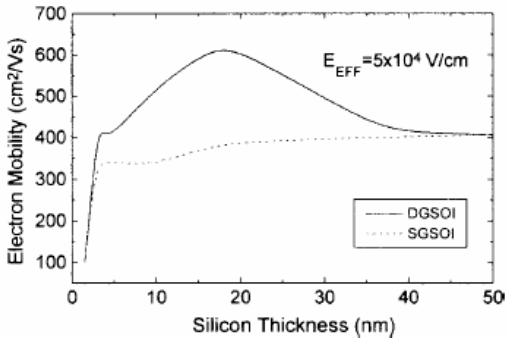

Fig-19: Evolution of electron mobility for a DGSOI (solid line) and a SGSOI (dashed line) with the thicknesses of the silicon layer. All the scattering mechanisms were taken into account.

It also shows the existence of the three following regions (see figure 19) . A first region for thick silicon slabs (T_w*:* 20– 30 nm), where mobility for both structures tends to coincide. For these thicknesses, an inversion layer near each interface is formed. Electrons in these inversion layers behave as they do in bulk or SGSOI inversion layers. As *Tw* decreases, an interaction between the two inversion layers is produced. As a result, the sub-band structure and wave functions are strongly modified with respect to bulk silicon inversion layers. As a consequence, electrons are spread throughout the silicon volume (volume inversion). We have shown that volume inversion modifies the electron transport properties by reducing the effect of all the scattering mechanisms. Accordingly, electron mobility in a DGSOI inversion is increased significantly. This increase depends on the silicon thickness and on the transverse effective field. Finally, for very small thicknesses, the limitations on electron transport are due to geometrical effects, and therefore the mobility in SGSOI and in DGSOI inversion layers, which again coincide, fall abruptly. This fact poses a serious limit to the minimum silicon thickness which can be used in these structures. Taking into account the contribution of the main scattering mechanisms, this limitation was estimated to be around 5 nm. In conclusion, there exists a range of silicon layer thicknesses in which electron mobility in DGSOI inversion layers is significantly improved as compared to bulk-silicon or SGSOI inversion layers.

f2. In the similar study done by Janik et al. [17], they also independently solved the semiconductor thickness effect on the electron concentration distribution and electron mobility, and found the strong dependence of both on semiconductor thickness. Considerations concern the whole range of the semiconductor thickness, from the bulk case to the ultra-thin range, where quantum effects become evident. Two approaches to the description of the semiconductor region are used—the “classical” model based on solution to the Poisson equation and the “quantum” model based on self-consistent solution to the Schrödinger and Poisson equation system (see figures 20 and 21) [14]. The semiconductor thickness effect on the electron effective mobility is considered with the use of the local mobility

model for the SOI transistors, based on the MINIMOS 5 mobility model [19], modified to the case of the SOI structure [20] (see figure 22).

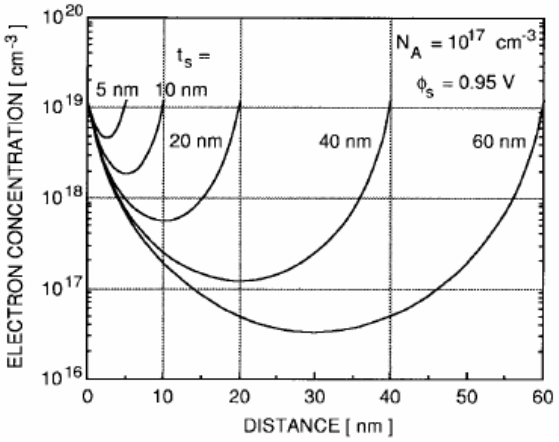

Fig-20: Influence of the semiconductor thickness on the electron concentration distribution at the surface potential constant according to the "classical" model.

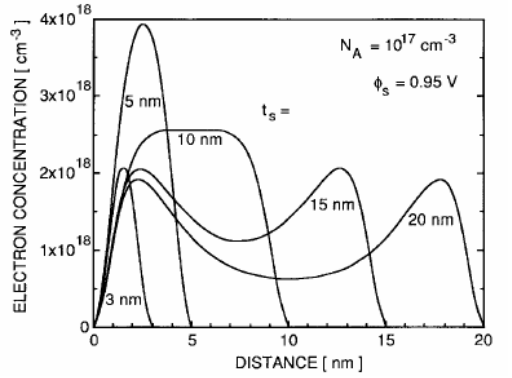

Fig- 21: Influence of the semiconductor thickness on the electron concentration distribution at the surface potential constant, according to the "quantum" model.

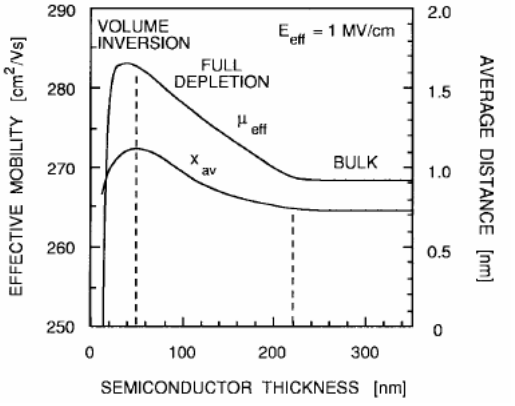

Fig- 22: Electron effective mobility in the symmetrical double-gate SOI transistor according to the classical" and "quantum" models of the semiconductor region and the local mobility model.

In dependence on the semiconductor layer thickness the double-gate SOI transistor can operate in various regimes: bulk, depletion, volume inversion, channels overlapping and the 2-DEG. The transition thicknesses depend on the dopant concentration and the gate voltage. For Na = 10^{17} cm^{-3} the transition between the depletion and volume inversion takes place at about 45 nm while the channel overlapping and the 2-DEG effects become important for thicknesses below 10 nm. For higher doping levels the transition thicknesses are smaller. The most advantageous semiconductor layer thicknesses for the GAA SOI transistor operation are near the onset of the volume inversion regime (i.e., about 50 nm), when the average distance of electrons from the surfaces is the largest and the effective mobility is the highest. Further reduction of the semiconductor thickness at the constant gate voltage results in an increase of the electron charge density with a simultaneous degradation of the effective mobility. For thickness less than 20 nm the latter effect becomes predominant. If the semiconductor thickness is smaller than about 10 nm (for Na = 10^{17} cm^{-3}), all negative effects superimpose: the two semiconductor surface regions containing most of electrons overlap causing a decrease of the electron charge density. The electron energy quantization additionally reduces the electron charge density and increases the threshold voltage. These effects combined with the mobility degradation result in a significant decrease of the drain current and degradation of the transfer characteristics of the transistor.

However, it is worth noticing that consideration of the semiconductor thickness effects on the double-gate SOI transistor performance was done without taking into account velocity saturation. Since the carrier saturation velocity usually presents a weaker dependence on the transverse electric field and scattering mechanisms than carrier mobility, the performance degradation resulting from the mobility decrease can be less significant for deep

submicron devices which operate in the velocity saturation regime [17].

Conclusion: Several processes to fabricate SOI wafers were discussed, and at present both SIMOX and UNIBOND techniques are viewed as future industrially scaled process. Advantages of SOI-MOSFETs with the stress on Double Gate MOSFETs were reviewed and technological challenges in realizing this new device structure were presented. Double Gate MOSFETs not only exhibit a near ideal sub-threshold slope but also provide short channel effect immunity which make them the ultimate scalable device structure.

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