Malay K Ganai

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Research Interests

- HW and SW systems verification, formal methods, verification methodology, automated error diagnosis, and constraint solvers.

Education

- Ph.D. Electrical & Computer Engineering, May 2001. University of Texas at Austin. *Dissertation: Algorithms for Efficient State Space Search*.
- M.S. Electrical & Computer Engineering, May 1998. University of Texas at Austin.
- B.Tech. Electrical Engineering, May 1992. Indian Institute of Technology, Kanpur, India.

Honors and Awards

- NECLA FY2006 Technology Commercialization Award for *F-Soft* Project, 2007.
- NECLA FY2005 Technology Commercialization Award for *VeriSol* Project, 2006.
- IBM CAS Fellowship, 1999.
- Best B.Tech. Project Award, EE Dept., IIT Kanpur, India 1992.
- TCS Excellence award for best CAD project, 1992.

Professional Experience

- **NEC Labs America,** Princeton, NJ. *Senior Research Staff Member*, May 2001- current
  - Developing efficient verification solution for concurrent systems
  - Developing distributed and scalable verification solution for software programs in *F-Soft*
  - Developed System Verification and Diagnosis Solutions in *F-Soft*
  - Principal architect and author of *VeriSol* (formerly *DiVer*), SAT-based Formal Verification platform available commercially as C-level property checker in NEC's CyberWorkBench Tool
- **IBM ARL**, Austin, TX. *Summer Intern*, 2000 & 2001.
  - Worked on Equivalence Checking tool *Verity*; devised on-the-fly compression algorithms for logical circuits
  - Verification of IBM designs using *SIVA tool.*
- **University of Texas at Austin,** TX. *Graduate Research Assistant*, Aug 1997-May 2001.
  - Developed integrated environment SIVA, a software tool based on semi-formal techniques for efficient state space search, used for hardware falsification.
- **Cadence Design Systems,** Noida, India. *Member of Technical Staff*, Nov 1995- July 1997.
  - Built fixed-point arithmetic libraries for SPW (signal processing workbench); cell characterization & modeling of ASIC libraries.
- **Larsen & Toubro Ltd,** Mysore, India: *Design Engineer*, Sep 1992 – Nov 1995.
  - Designed and developed electronic tri-vector meter.

Professional Activities

- **Technical Program Committee:** FMCAD (2006), DATE (2008), ICCAD(2008), PDMC (2008), SAC (2009)
- **Journal Article Reviews**: TCAD, STTT, TC, TODAES
- **Conference Paper Reviews**: DAC, FMCAD, ICCAD, ICCD, HVC, DATE, PDMC, SAC
- **Tutorial Organizer**: ICCAD (2008)
- **IEEE**
  - Senior Member
  - METSAC representative: 2008-present

Book(s)

- Malay K. Ganai and Aarti Gupta. SAT-based Scalable Formal Verification Solutions, Springer Science and Business Media, 2007.

Patents issued

- US 7,386,818 June 10, 2008. "Efficient modeling of embedded memories in bounded model checking"
- US 7,346,486 Mar 18, 2008. "System and method for modeling, abstraction, and analysis of software"
- US 7,305,637 Dec 04, 2007. "Efficient SAT-based unbounded symbolic model checking"
- US 7,203,917, Apr 10, 2007. "Efficient distributed SAT and SAT-based distributed bounded model checking".
- US 6,473,884, Oct 02, 2002. "Method and system for equivalence-checking combinatorial circuits using iterative binary-decision-diagram sweeping and structural satisfiability analysis"

Patents Pending

- US 20080281563: "Modeling and Verification of Concurrent Systems using SMT-based BMC"
- US 20070226666: "High-level Synthesis for Efficient Verification"
- US 20070226665: "Accelerating High-level Bounded Model checking":
- US 20060282806: "Software verification using range analysis"
- US 20060282807: "Software Verification".
- US 20040230407: "Iterative abstraction using SAT-based BMC with proof analysis"
- US 20030225552: "Efficient approaches for bounded model checking"

Tutorials

- "Embedded Software Verification: Challenges and Solution" ICCAD, Nov 2008
- "Verification of C-based Design" (Part of tutorial entitled "C-based Design: Industry Experience"), ASPDAC, Jan 2005.

Papers in Refereed Journals

1. Franjo Ivančić, Zijiang Yang, Malay K. Ganai, Aarti Gupta, and Pranav Ashar: Efficient SAT-based Bounded Model Checking for Software Verification, Journal on Theoretical Computer Science (TCS), Volume 404(3), September 2008, pages 256-274, Elsevier.

2. Aleksandr Zaks, Zijiang Yang, Ilya Shlyakhter, Franjo Ivančić, Srihari Cadambi, Malay K. Ganai, Aarti Gupta, and Pranav Ashar: Bitwidth Reduction via Symbolic Interval Analysis for Software Model Checking, Transactions Brief Paper in the IEEE Transactions on CAD, volume 27(8), Aug. 2008, pages 1513-1517, IEEE.

3. Malay K. Ganai, Muralidhar Talupur, Aarti Gupta: SDSAT: Tight Integration of Small Domain Encoding and Lazy Approaches in Solving Difference logic. JSAT 91-114 (June 2007).
4. Malay K. Ganai, Aarti Gupta, Zijiang Yang, Pranav Ashar: Efficient distributed SAT and SAT-based distributed Bounded Model Checking. STTT 8(4-5): 387-396 (2006)
5. Andreas Kuehlmann, Viresh Paruthi, Florian Krohm, Malay K. Ganai: Robust Boolean reasoning for equivalence checking and functional property verification. IEEE Trans. on CAD of Integrated Circuits and Systems 21(12): 1377-1394 (2002)
6. Malay K. Ganai, Praveen Yalagandula, Adnan Aziz, Andreas Kuehlmann, Vigyan Singhal: SIVA: A System for Coverage Directed State Space Search. JETTA, 2001.

Papers in Refereed Conferences and Workshops

1. Malay K Ganai. Efficient Efficient Decision Procedure for Bounded Integer Non-linear Operations using SMT(LIA). HVC 2008
2. Malay Ganai and Weihong Li. *D-TSR*: Parallelizing SMT-based BMC using Tunnels over Distributed Framework. HVC 2008. (Tool paper)
3. Gogul Balakrishnan and Malay K. Ganai. Proof-guided Error Diagnosis by Triangulation of Program Error Causes. SEFM 2008.
4. Malay K. Ganai, Aarti Gupta: Efficient Modeling of Concurrent Systems in BMC. SPIN 2008: 114-133
5. Sudipta Kundu, Malay K. Ganai, Rajesh Gupta: Partial order reduction for scalable testing of systemC TLM designs. DAC 2008: 936-941
6. Malay K. Ganai, Aarti Gupta: Tunneling and slicing: towards scalable BMC. DAC 2008: 137-142
7. Malay K. Ganai, Aarti Gupta: Completeness in SMT-based BMC for Software Programs. DATE 2008: 831-836.
8. Malay K. Ganai, Aarti Gupta, Franjo Ivančić, Vineet Kahlon, Weihong Li, Nadia Papakonstantinou, Sriram Sankaranarayanan, and Chao Wang: Towards Precise and Scalable Verification of Embedded Software**,** *2008 Design and Verification Conference (DVCon)*, San Jose, CA, February 2008 (invited paper).
9. Malay K. Ganai, Akira Mukaiyama, Aarti Gupta, Kazutoshi Wakabayashi: Synthesizing "Verification-aware" Models: Why and How? VLSI Design 2007.
10. Malay K. Ganai, Aarti Gupta: Efficient BMC for Multi-clock Systems with Clocked Specifications: ASPDAC 2007.
11. Malay K. Ganai, Aarti Gupta: Accelerating High-level Bounded Model Checking. ICCAD 2006.
12. Malay K. Ganai, Akira Mukaiyama, Aarti Gupta, Kazutoshi Wakabayashi: Another Dimension to High-level Synthesis: Verification? DCC Workshop, 2006
13. Chao Wang, Aarti Gupta, Malay K. Ganai: Predicate learning and selective theory deduction for a difference logic solver. DAC 2006: 235-240
14. Malay K. Ganai, Muralidhar Talupur, Aarti Gupta: SDSAT: Tight Integration of Small Domain Encoding and Lazy Approaches in a Separation Logic Solver. TACAS 2006: 135-150

15. Chao Wang, Franjo Ivancic, Malay K. Ganai, Aarti Gupta: Deciding Separation Logic Formulae by SAT and Incremental Negative Cycle Elimination. LPAR 2005: 322-336

16. Malay K. Ganai, Aarti Gupta, Pranav Ashar: Beyond safety: customized SAT-based model checking. DAC 2005: 738-743

17. Malay K. Ganai, Aarti Gupta, Pranav Ashar: Verification of Embedded Memory Systems using Efficient Memory Modeling. DATE 2005: 1096-1101

18. Malay K. Ganai, Aarti Gupta, Pranav Ashar: DiVer: SAT-Based Model Checking Platform for Verifying Large Scale Systems. TACAS 2005: 575-580

19. Aarti Gupta, Malay K. Ganai, Pranav Ashar: Lazy Constraints and SAT Heuristics for Proof-Based Abstraction. VLSI Design 2005: 183-188

20. Franjo Ivancic, Zijiang Yang, Malay K. Ganai, Aarti Gupta, Ilya Shlyakhter, Pranav Ashar: F-Soft: Software Verification Platform. CAV 2005: 301-306

21. Franjo Ivancic, Ilya Shlyakhter, Aarti Gupta, Malay K. Ganai: Model Checking C Programs Using F-SOFT. ICCD 2005: 297-308

22. Himanshu Jain, Franjo Ivancic, Aarti Gupta, Malay K. Ganai: Localization and Register Sharing for Predicate Abstraction. TACAS 2005: 397-412

23. Malay K. Ganai, Aarti Gupta, Pranav Ashar: Efficient Modeling of Embedded Memories in Bounded Model Checking. CAV 2004: 440-452

24. Malay K. Ganai, Aarti Gupta, Pranav Ashar: Efficient SAT-based unbounded symbolic model checking using circuit cofactoring. ICCAD 2004: 510-517

25. Aarti Gupta, Malay K. Ganai, Chao Wang, Zijiang Yang, Pranav Ashar: Abstraction and BDDs Complement SAT-Based BMC in DiVer. CAV 2003: 206-209

26. Malay K. Ganai, Aarti Gupta, Zijiang Yang, Pranav Ashar: Efficient Distributed SAT and SAT-Based Distributed Bounded Model Checking. CHARME 2003: 334-347

27. Aarti Gupta, Malay K. Ganai, Chao Wang, Zijiang Yang, Pranav Ashar: Learning from BDDs in SAT-based bounded model checking. DAC 2003: 824-829

28. Aarti Gupta, Malay K. Ganai, Zijiang Yang, Pranav Ashar: Iterative Abstraction using SAT-based BMC with Proof Analysis. ICCAD 2003: 416-423

29. Malay K. Ganai, Adnan Aziz: Improved SAT-based Bounded Reachability Analysis. ASP-DAC 2002: 729-734 (also appeared in VLSI Design 2002).

30. Malay K. Ganai, Pranav Ashar, Aarti Gupta, Lintao Zhang, Sharad Malik: Combining strengths of circuit-based and CNF-based algorithms for a high-performance SAT solver. DAC 2002: 747-750

31. Andreas Kuehlmann, Malay K. Ganai, Viresh Paruthi: Circuit-based Boolean Reasoning. DAC 2001: 232-237 (nominated for best paper)

32. Malay K. Ganai, Adnan Aziz: Rarity based guided state space search. ACM Great Lakes Symposium on VLSI 2001: 97-102

33. Malay K. Ganai, Andreas Kuehlmann: On-the-fly Compression of Logical Circuits. IWLS, 2000.

34. Tai-Hung Liu, Malay K. Ganai, Adnan Aziz, Jeffrey L. Burns: Performance Driven Synthesis for Pass-Transistor Logic. VLSI Design 1999: 372-377

35. Malay K. Ganai, Adnan Aziz: Enhancements to Invariant Verification using SIVA. HLDVT 1999.

36. Malay K. Ganai, Adnan Aziz, Andreas Kuehlmann: Enhancing Simulation with BDDs and ATPG. DAC 1999: 385-390

37. Malay K. Ganai, Adnan Aziz: Efficient Coverage Directed State Space Search. IWLS, 1998.