# A digital engineering curriculum for the new millennium

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**Abstract** This paper examines the development of a digital engineering curriculum, which closely integrates EDA tools and multimedia courseware into the syllabus. It describes the software that has been integrated, including tools for schematic capture, logic simulation, VLSI design and high-level simulation and highlights the advantages of closely integrating computer-based teaching with conventional lecture-based material.

**Keywords** computer-based teaching; digital engineering

## Introduction

The last decade of the twentieth century has seen tremendous technological advances in the digital arena. This progress is reflected in many inter-related areas, for example:

- Advanced fabrication processes that allow complete systems to be built on a single chip;
- The computational power of microprocessors;
- The increasing capacity of storage devices and digital media;
- The convergence of digital communications with media and computing resources.

Not surprisingly, these developments have had a substantial impact on the digital engineering curriculum taught at universities and, indeed, on the way the material is presented to students. In particular, an integral component of any such curriculum is the use of computer-aided design (CAD) tools for digital design and analysis. With the advent of comparatively cheap yet powerful PC workstations, use of these tools can not only be very closely integrated into engineering courses, but computer-based learning (CBL) courseware can also be used to augment the student's learning experience whilst using these tools.

This paper describes the *'Year 2000 Ready'* Digital Engineering curriculum at the University of Kent, which has recently been developed for students on the Computer and Electronic Systems Engineering programmes, and closely integrates EDA tools and multimedia courseware into the syllabus.

In the late 1990s, there was a large-scale move by the University Computing Service to the Windows NT operating system, largely for reasons of security and networked account management. It was therefore necessary for the Electronic Engineering Department not only to mirror this move so that our students could continue to make use of university facilities, but also to identify new electronic design automation (EDA) tools and incorporate them into the

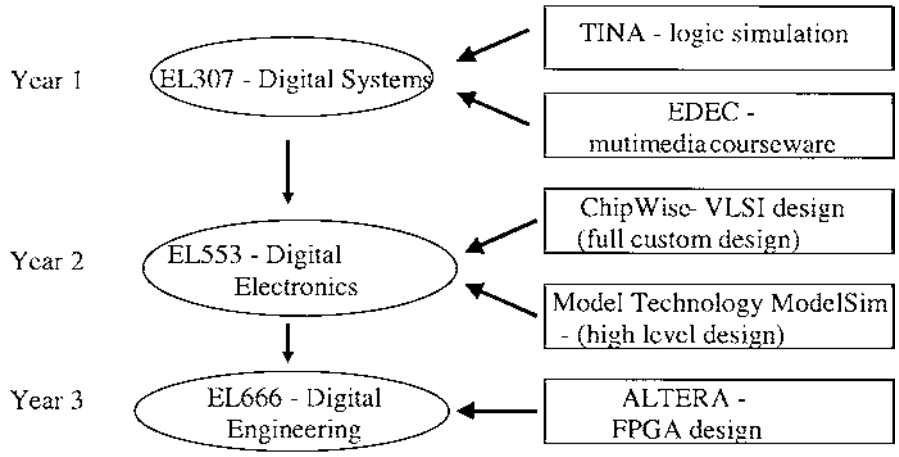


Fig. 1 *Digital Engineering Curriculum and EDA Tools.*

syllabus. The result of this process is summarized in Fig. 1, which shows the relationship between the EDA tools and the course components of the Digital Engineering curriculum.

### First-year syllabus

The academic year at Kent is structured into eight course unit modules. The Digital Systems module is the main unit concerned with Digital Engineering in the first year and has been designed so that students will have the necessary theoretical background to understand the operation of large-scale digital systems. The main aims are for students to develop the necessary skills to enable them to design, in a structured way, the logic of moderately complex digital systems and to become familiar with the capabilities and operation of digital CAD tools. These aims are achieved by means of lectures, simulation exercises, design laboratory experiments and by using CBL courseware. *Digital Systems* covers the following material:

- *Introduction to Logic Systems*, which introduces the topics of simple logic gates, Karnaugh maps, functional building blocks such as adders and comparators, and the use of behavioural descriptions to describe the behaviour of logic blocks.
- *Logic System Design*, covering the topics of shift registers and the building of asynchronous and synchronous counters.
- *Sequential Machine Design*, covering the topics of finite state machines, Mealy and Moore machines, state reduction and ASM charts.
- *Digital Logic Implementation*, which introduces the use of programmable logic devices, field programmable gate arrays (FPGAs) and the design of VLSI structures.

Table 1 *Teaching and learning contact hours for Digital Systems*

| Lectures | Simulation exercises | Multimedia courseware | Laboratory experiments |
|---|---|---|---|
| 35 hours | 12 hours | 4 hours | 5 hours |

The lectures are augmented by fortnightly sessions, each lasting 2 hours, on the PC, where the students take a range of circuit design and computer-based exercises using TINA Pro (Toolkit for Interactive Network Analysis). Students are also given access to CBL material from the Electronics Design Education Consortium (EDEC). TINA and EDEC are described further below.

Finally students gain practical experience with a laboratory-based experiment where they design and implement a small-scale digital system.

The distribution of teaching and learning activities in the module, which we believe provides the optimum balance, is shown in Table 1.

The 35 lectures provide a foundation to the module, which is enhanced by the simulation exercises and multimedia courseware. In addition we like the students to get hands-on experience of digital hardware development. To this end, we provide the one-day laboratory experiment described earlier.

We have found this combination of teaching highly successful, in that student feedback is very good, as is performance in end-of-year examinations. Students are highly motivated which helps to ensure that our key objectives, of laying a firm foundation in logic system design and a solid comprehension of design principles, are attained.

### First-year EDA tools

Assignments using TINA Pro[1] form a central part of our first-year teaching. TINA Pro includes schematic capture for circuitry entry, a comprehensive library of components and both digital and analogue simulation. The software is installed on a server in the Electronic Engineering Laboratory, and accessed from networked PCs under the Windows NT operating system. Because the tools also support analogue simulation, TINA is used for other course units in the programme. The tools are extremely easy to use, with the result that experiments now take half the time to run compared with the tools used in previous years.

Figures 2 and 3 show the schematic and simulation using TINA of a FSM design, which is one of the experiments used in the first-year course.

The CBL courseware was developed by the Electronics Design Education Consortium (EDEC),[2] a consortium of eight universities — UMIST, Manchester, Bristol, Kent, Essex, Newcastle, Oxford Brookes and Huddersfield. The courseware consists of multimedia material that allows a student to proceed through the courseware at a pace best suited for that individual. A typical module consists of text, graphics, animations and interaction. This type of material is particularly successful in getting across concepts that are difficult to comprehend in just a lecture presentation.

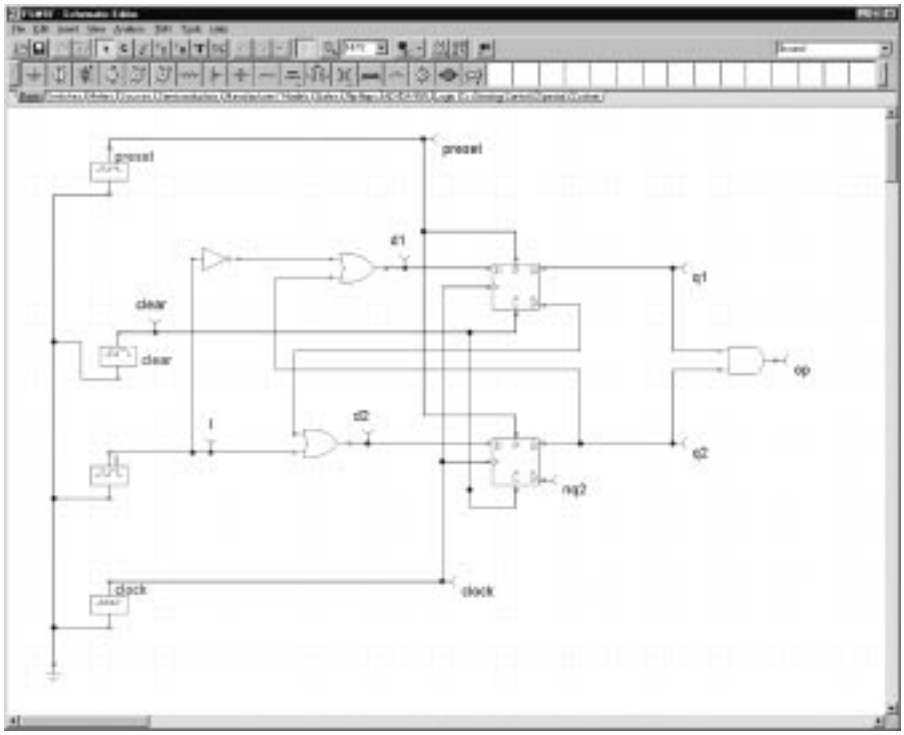


Fig. 2 *FSM design using TINA.*

## Second-year syllabus

The *Digital Electronics* course unit is concerned with both the low-level and high-level design of digital integrated circuits. Low-level physical design is used in both cell design as well as mixed-signal design, whilst synthesis from VHDL has become the method of choice for designing digital systems. These two aspects are covered by the following two components:

- *Digital Technologies and VLSI.* This examines digital circuits implemented in different technologies such as CMOS, ECL and TTL, and the design of CMOS VLSI circuits. An integral component of the course is a set of computer-based assignments using the ChipWise Tutor courseware, a CBL system for VLSI design training which is described below.
- *Introduction to VHDL.* This course introduces a subset of the language and enables moderately complex behavioural and structural models of digital components to be developed. Practical work associated with this component is performed on PCs using Model Technology's ModelSim VHDL compiler and simulator.[3]

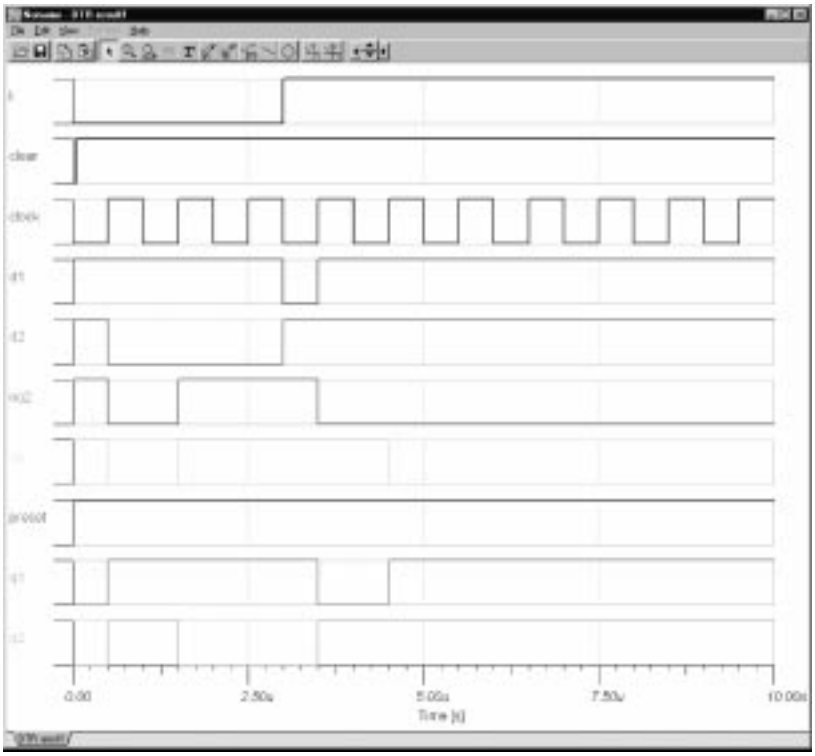

Fig. 3 *FSM design simulated using TINA.*

### Using ChipWise Tutor

ChipWise Tutor[4] is a novel World Wide Web (WWW)-based CBL system for VLSI design where the courseware authored in hypertext mark-up language (HTML) has the ability to control the ChipWise VLSI CAD system.[5] Figure 4 shows a screen shot, where you can see the design system ChipWise on the left-hand side and the Netscape Navigator WWW browser[6] on the right. Pressing a hyper link embedded in the courseware operates the design system. Using ChipWise Tutor, the student obtains proficiency in using a moderately complex and powerful design system and gains an insight into practical VLSI circuit design and layout. The courseware, which has been designed to occupy students for two lab days, is composed of seven modules:

- An Introduction to ChipWise
- Transistor Sizing
- Simple Logic Gates
- The Dynamic Shift Register
- The Parallel Load Shift Register
- The 4 to 1 multiplexer
- Parity Generation

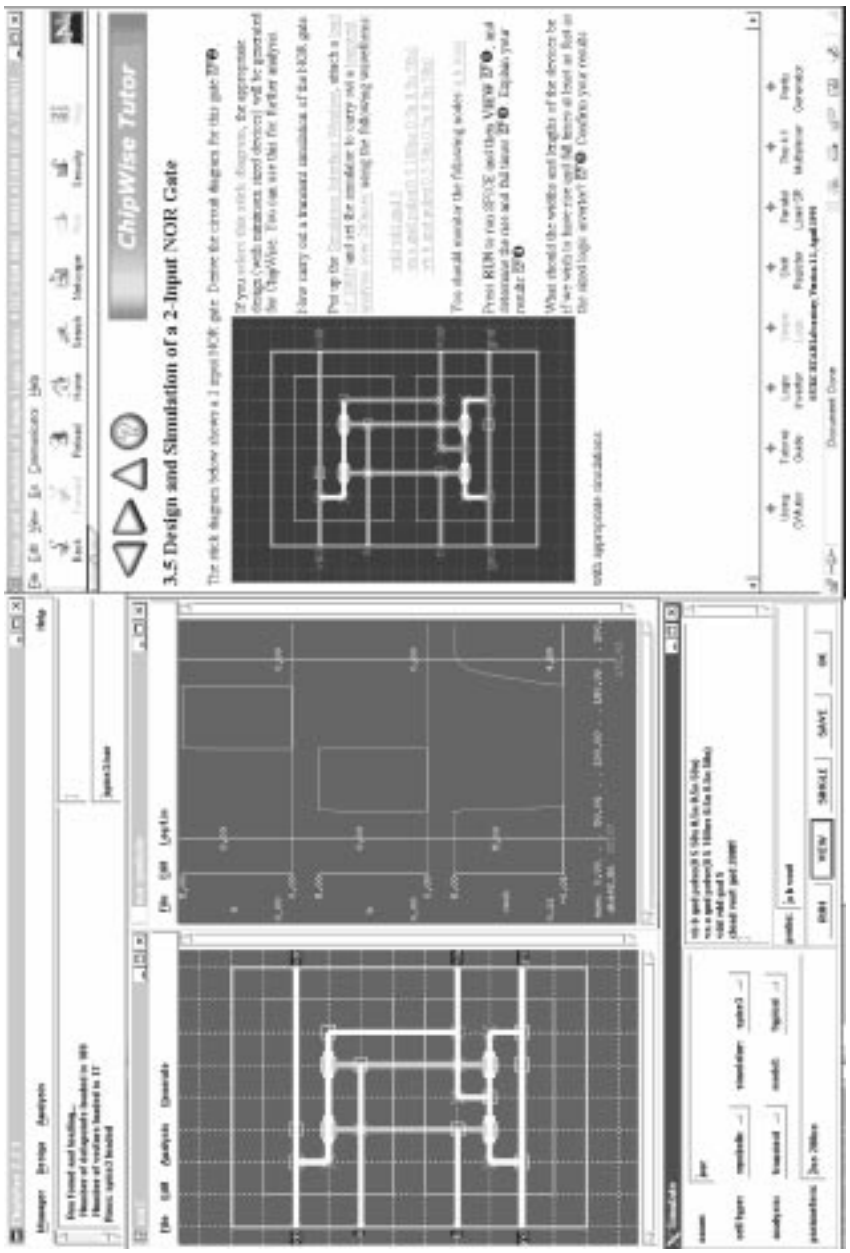


Fig. 4 *Screen-shot of ChipWise Tutor.*

### Assignments using ModelSim

The second-year VHDL course aims to provide students with an understanding of the key features of VHDL. Throughout the course there are a graduated set of examples which students undertake to gain familiarity and fluency with the language. For the most part these involve modifying and/or extending designs introduced in the lectures. Once this familiarity has been developed a 1-day design experiment is undertaken. In this, students design a pulse-position modulation, data communications system. This has to be modelled at as high a level of abstraction as possible, i.e. the use of integer-based counters and comparators, etc., rather than designing in logic gates. This emphasis has been adopted so that students are prepared for high-level design with synthesis tools.

## Third-year syllabus

In the third year, the main aim is the examination of the problems and methodology of designing and implementing large digital systems. Implementation methods include fixed instruction set microcomputers, programmable and random logic and semi and full custom integrated circuits. In recognition of the fact that so many digital systems are now implemented with field programmable gate arrays (FPGAs), a lecture course has been developed specifically in this area. Typical FPGA architectures are reviewed including a discussion of granularity, methods of interconnection and programming techniques. Design techniques for FPGAs, such as finite-state machine encoding, high-speed counter and adder design are explored. Consideration is also given to the VHDL coding style that makes best use of high-level synthesis tools.

At this advanced level, practical experience integrated with the lectures is a key component. Hence this unit includes 20 hours of PC-based synthesis and FPGA design exercises which are discussed below.

### VHDL extended project

An extended VHDL project is taken in the third year where students are given the details of the instruction set of a processor and a set of systems components described in VHDL. These include a program counter register, instruction register, dual port register file, memory, ALU and control unit. The architecture of the complete processor is illustrated in Fig. 5. They first examine the behaviour of each component and combine them into a processor. The taxing part of the project is to extend the control unit. The supplied version of the control unit has only a small number of instructions implemented, sufficient to act as an explanation of the operation of the control unit. Students then have to develop extra instructions including a subroutine call and return facility.

### Structured VHDL assignments

The other activity involves the use of the Altera MAX + PlusII system.[7] We have developed a general-purpose board, shown in Fig. 6, that employs a MAX8000 device. This has a number of other general-purpose components,

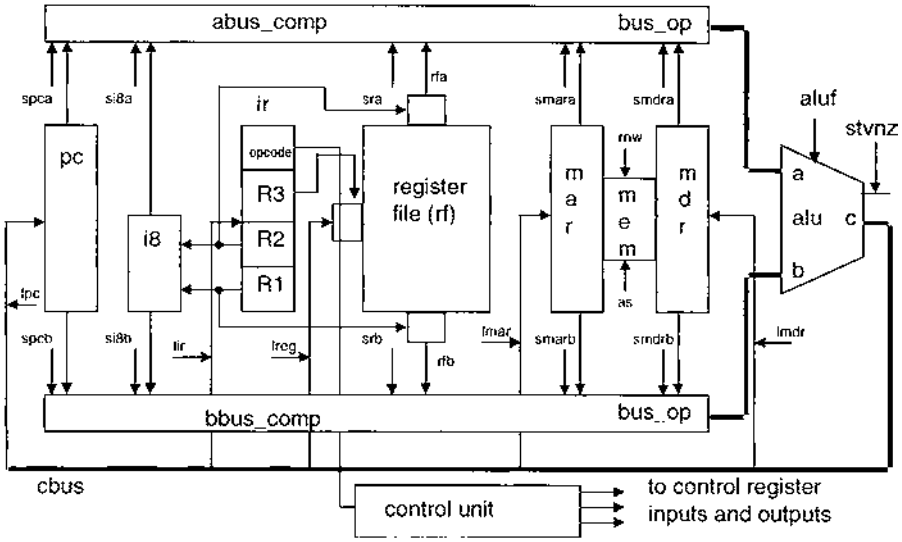


Fig. 5 *VHDL Assignment Processor.*

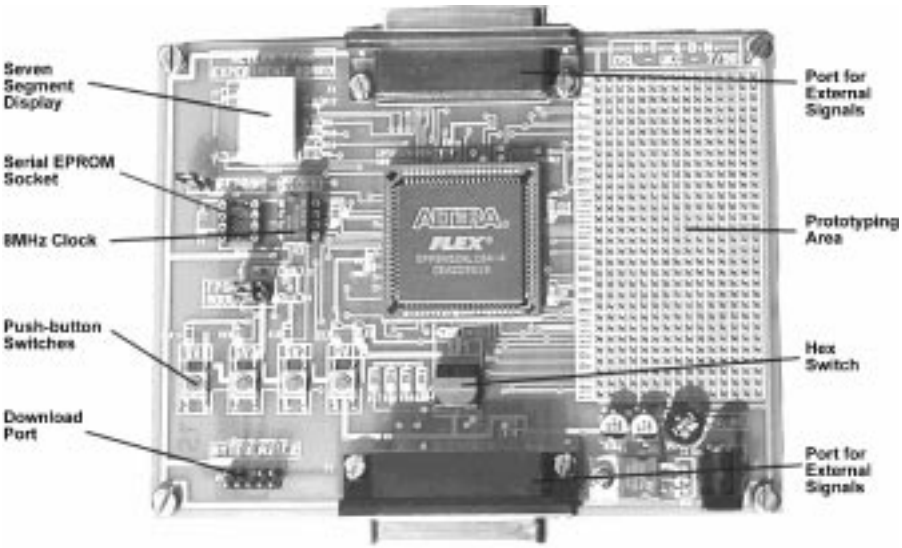


Fig. 6 *Altera Prototyping Board for Synthesis Assignments.*

RAM, seven-segment displays, switches and D/A converter. The board is organised so all these devices are connected via drivers to a common bus. This makes it relatively simple to vary the flow of information. The activity with this equipment is to develop an interval timer. The reference clock source is 16 MHz and thus this has to be divided down to the 1 s rate.

A finite-state machine controls the function of the timer. A key feature of the design is that it has to be totally synchronous in operation. This reinforces the material presented in the associated lecture course.

## Evaluation

The main evaluation of CBL methods that we have undertaken is in the context of its introduction into the second-year Digital Electronics unit where students spend two laboratory days using the ChipWise Tutor system. Here, we found that students make good progress through the courseware, have far fewer problems with the software than in the past and usually complete six of the seven modules within the allotted time. We have issued courseware evaluation forms in an attempt to gauge the success or otherwise of using this type of material. The results of this evaluation have been reported in Ref. 4. In summary, students consider that this is an interesting form of teaching and that they have learnt a great deal about VLSI design. The questions concerned with productivity of the courseware compared with lecture classes reveal that they consider this type of teaching to be an enhancement of a lecture course rather than a replacement of lectures.

## Conclusions

The move by the University Computing Service to the Windows NT operating system has given us the opportunity of constructing a *'Year 2000 Ready'* Digital Engineering curriculum, which closely integrates both EDA tools and high-quality CBL courseware into the syllabus. Availability and exposure to the software is excellent since the tools and courseware are PC based. The EDA tools are extremely easy to use, whilst the EDEC courseware and ChipWise Tutor are both very effective at illustrating lecture material and therefore popular with students. It is interesting to note that it would have been impossible to construct a similarly profiled curriculum using software on the more traditional (and expensive) UNIX platform.

## Acknowledgements

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## Abstracts — French, German, Spanish

**Un cursus d'ingénierie numérique pour le nouveau millénaire**
Cet article examine le développement d'un cursus en ingénierie numérique qui intègre intimement les outils EDA et le matériel d'enseignement par multimédia dans le syllabus. Il décrit le logiciel qui a été intégré y compris les outils pour la saisie de schémas, la simulation logique, la conception et la simulation de haut niveau de VLSI et met en évidence les avantages d'une intégration poussée de l'enseignement basé sur ordinateur avec des cours basés sur des exposés conventionnels.

**Ein Lehrplan für Digitaltechnik für das neue Jahrtausend**
Dieser Bericht untersucht die Entwicklung eines Lehrplans für Digitaltechnik, die EDA Werkzeuge und Multimedienkursmaterialien in den Lehrplan einbaut. Er beschreibt die integrierte Software, sowie die Werkzeuge für schematische Erfassung, Logiksimulation, VLSI (Größtintegration) Design und Hochpegelsimulation und hebt die Vorteile des genau integrierenden Lehrens auf Computerbasis mit herkömmlichen, auf Vorlesungen basierendem Material hervor.

**Curriculum en ingeniería digital para el nuevo milenio**
Este artículo examina el desarrollo de un curriculum en ingeniería digital, que integra muy estrechamente herramientas EDA y material de curso multimedia en su programa. Describe el software que ha sido integrado, incluyendo herramientas para la captura automática de esquemáticos, simulación lógica, diseño VLSI y simulaciones de alto nivel y resalta las ventajas de integrar estrechamente enseñanzas basadas en ordenador junto con material empleado en clases convencionales.