26.8 A 2GHz CMOS Variable-Gain Amplifier with 50dB Linear-in-Magnitude Controlled Gain Range for 10GBase-LX4 Ethernet

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The standard of next-generation gigabit Ethernet, 10GBase-LX4 Ethernet, was finalized in 2003 and is emerging into network markets [1]. 10GBase-LX4 Ethernet employs wavelength division multiplexing (WDM) to carry different channels on different wavelengths on a bundled fiber. 8B/10B coding scheme is deployed to ensure transmission quality. Figure 26.8.1 shows the sophisticated implementation of 10GBase-LX4 Ethernet system. Each channel carries 3.125Gb/s data after optical demultiplexing, and its own individual optical receiver circuits. This mandates a wideband variable gain amplifier (VGA) with wide controlled gain range. The VGA poses challenging constraints, such as bandwidth, tuning range, etc. The VGA reported here demonstrates a 2GHz bandwidth with 50dB linear-controlled gain range, which is the widest bandwidth reported in CMOS technology to date to the authors' knowledge.

Figure 26.8.2 depicts the proposed variable gain amplifier with post amplifiers and dc offset canceling networks. It consists of a VGA, a five-stage post amplifier, an offset extraction circuit, and the output buffer. The gain of the VGA is linear-in-magnitude controlled by the control voltage V_c over a wide tuning range. The five-stage post amplifier affords sufficient voltage gain to increase the sensitivity. The offset cancellation circuit exhibits a negative feedback low-pass filter to eliminate the dc offset voltage due to device mismatch. A high-speed output buffer is mandated to drive off-chip loads.

The gain cell of the post amplifier adopts MOS-L as loads to extend bandwidth [2]. Each gain cell provides 6dB voltage gain, and achieves a bandwidth exceeding 10GHz. The offset cancellation circuit consists of an offset subtractor and a low-pass filter. The offset subtractor is fully differential to mitigate dc offset and meanwhile provides 6dB voltage gain with active inductor peaking. To meet a lower 3dB frequency requirement, the resistor and capacitor values in the low-pass network must be very large and occupy significant chip area. To minimize chip area, a PMOS transistor operating in the triode region is employed as the resistor, whose resistance is inversely proportional to its channel width. The capacitor is realized as an NMOS transistor which has its drain, source, and body connected to ground. The low-pass filter, shown in Fig. 26.8, is designed for a lower cut-off frequency of 300kHz. Output buffer is responsible for delivering a large current to drive off-chip loads at 3.125Gb/s. As shown in Fig. 26.8.2, the buffer consists of two stages. To attain sufficient output swing for succeeding decision circuits, the tail current of the last stage is designed as 5mA to provide 500mV differential output swing. Inductive peaking is deployed to ameliorate severe parasitic capacitance introduced by larger active device feature sizes.

To achieve the linear relationship between the VGA voltage gain and the control voltage V_C, the Gilbert type four-quadrant multiplier, depicted in Fig. 26.8.3a, is used since its output is equal to the product of the two inputs [3]. The analytic relationship between input and output is derived as follows.

$$\begin{aligned} V_{O+} - V_{O-} &= (g_{m3,4} - g_{m5,6}) \cdot R \cdot (V_{in+} - V_{in-}) \\ &= \sqrt{\frac{k_n'\left(W/L\right)}{2I_{SS}}} \cdot g_{m1,2}(V_{C+} - V_{C-})(V_{in+} - V_{in-}) \end{aligned} \quad (1)$$

Assume all transistors operate at saturation mode, i.e. the three differential pairs work as linear transconductors. However, there are two drawbacks which make it difficult to implement this VGA using the Gilbert cell. First, the cascode structure requires large voltage headroom and has difficulty functioning well with a 1.8V supply. Observe that the feedback loop of the AGC system works at very low speed; thus the control voltage varies at a very slow rate. Figure 26.8.3b depicts the proposed folded Gilbert cell, where the bottom differential pair of the original Gilbert cell can be folded without degrading its performance to reduce the number of cascoded transistors. Second, the voltage gain of the VGA changes its polarity as the control voltage changes. This limits the tuning range of the control voltage. To extend the linear control range, a constant current source which sinks a current slightly greater than I_{SS}, is added to the tail of one of the differential pairs to force one differential pair to possess a gain higher than the other's over the entire control range.

This VGA is implemented in 0.18μm CMOS technology and measured in chip-on-board assemblies. Figure 26.8.4 shows the die micrograph. Miniature 3D inductors are deployed in the output buffer to further minimize die area [4]. 3D inductors exhibit a higher self-resonant frequency at larger inductance values. The active area is 0.7mm^2 including PADs.

Figure 26.8.5a shows the measured S21 with different control voltage from -0.5V to 0.5V in steps of 0.2V. The measured S21 varies from 21dB to -11dB, and the upper 3dB frequency is 2GHz. After obtaining the measured S parameters, the voltage gain, A_v, can be transformed using Eq. (2).

$$A_v = \frac{2S_{21}}{(1+S_{11})(1-S_{22}) + S_{21}S_{12}} \quad (2)$$

which shows the differential midband voltage gain is from -16dB to 34dB. The measure voltage gain as a function of control voltage V_c has depicted in Fig. 26.8.5b, revealing linear-in-magnitude gain transfer characteristic in V_c from -0.4V to +0.4V.

Figure 26.8.6 depicts the measured BER vs. input signal amplitude and output eye diagrams at 3.125Gb/s 2^{31}-1 random sequence for $9mV_{pp}$, $20mV_{pp}$, and $495mV_{pp}$, respectively. The measured dynamic range is 35dB, from $9mV_{pp}$ to $495mV_{pp}$, indicating BER<10^{-12}.

Figure 26.8.7 summarizes the measured performance. This fully integrated work achieves 2GHz bandwidth and 50dB linear control range in CMOS technology.

Acknowledgements:
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References:

[1] IEEE Std. 802.3af-2003.
[2] E. Säckinger, and W. C. Fischer, "A 3-GHz 32-dB CMOS Limiting Amplifier for SONET OC-48 Receiver," *IEEE J. Solid-State Circuits,* vol. 35, no. 12, pp. 1884-1888, Dec. 2000.
[3] B. Gilbert, "A Precise Four-Quadrant Multiplier with Subnanosecond Response," *IEEE J. Solid-State Circuits,* vol. SC-3, pp. 365-373, Dec. 1968.
[4] C.-C. Tang, C.-H. Wu, and S.-I. Liu, "Miniature 3D Inductors in Standard CMOS Process," *IEEE J. Solid-State Circuits*, vol. 37, pp. 471-480, April 2002.

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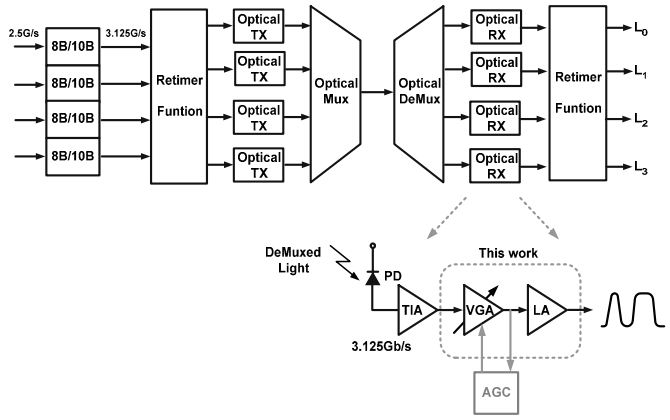

Figure 26.8.1: System diagram of a 10GBase-LX4 ethernet.

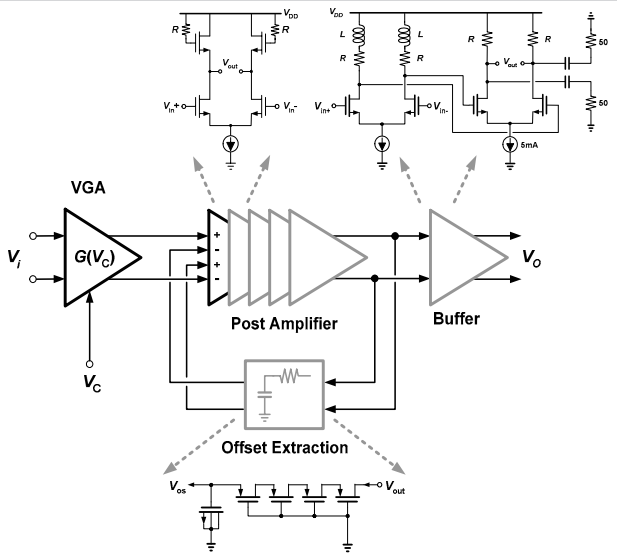

Figure 26.8.2: Proposed low voltage VGA topology and subcircuit schematic.

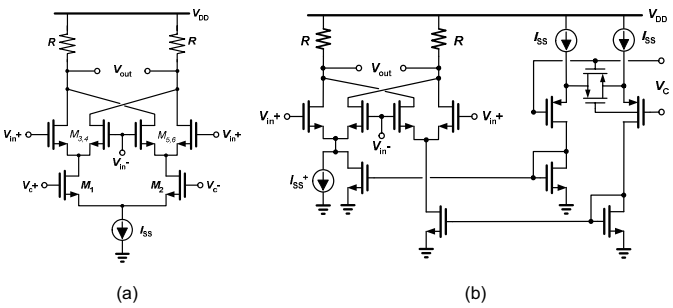

Figure 26.8.3: Circuit schematics (a) Conventional Gilbert cell (b) Proposed folded VGA structure.

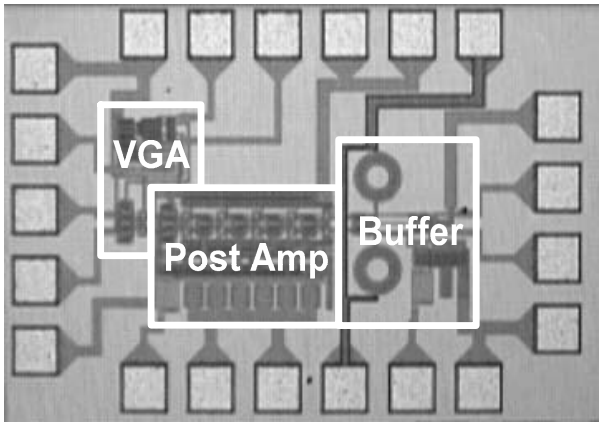

Figure 26.8.4: Die photo of the 3.125Gb/s VGA.

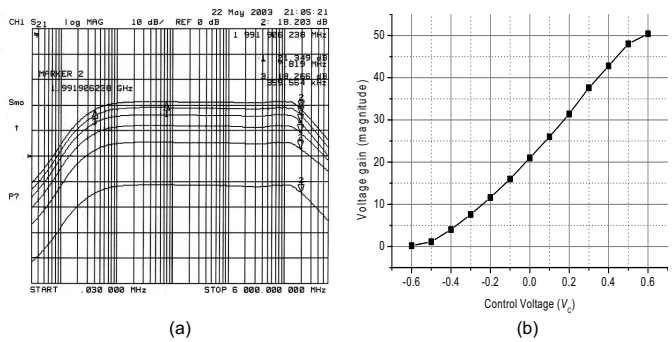

Figure 26.8.5: Measure frequency response (a) S21 (V_c: -0.5V to 0.5V, step: 0.2V from bottom to top) (b) voltage gain vs. control voltage V_c.

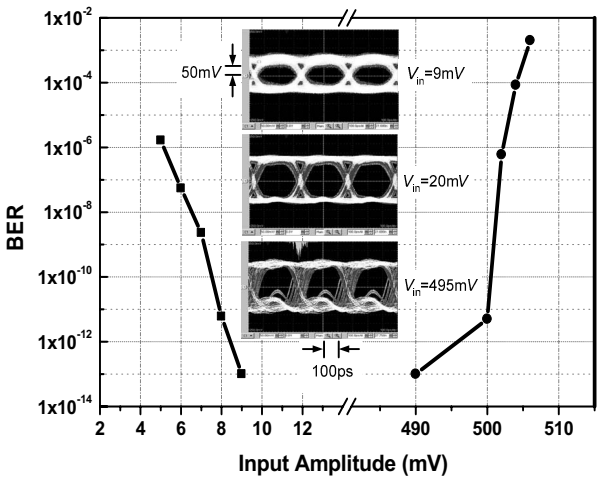

Figure 26.8.6: Measured BER vs. input signal amplitude and eye diagrams at 3.125Gb/s 2^{31}-1 PRBS data for input peak-to-peak signal level 9mV, 20mV, and 495mV, respectively (Horizontal scale: 100ps/div, Vertical scale: 50mV/div).

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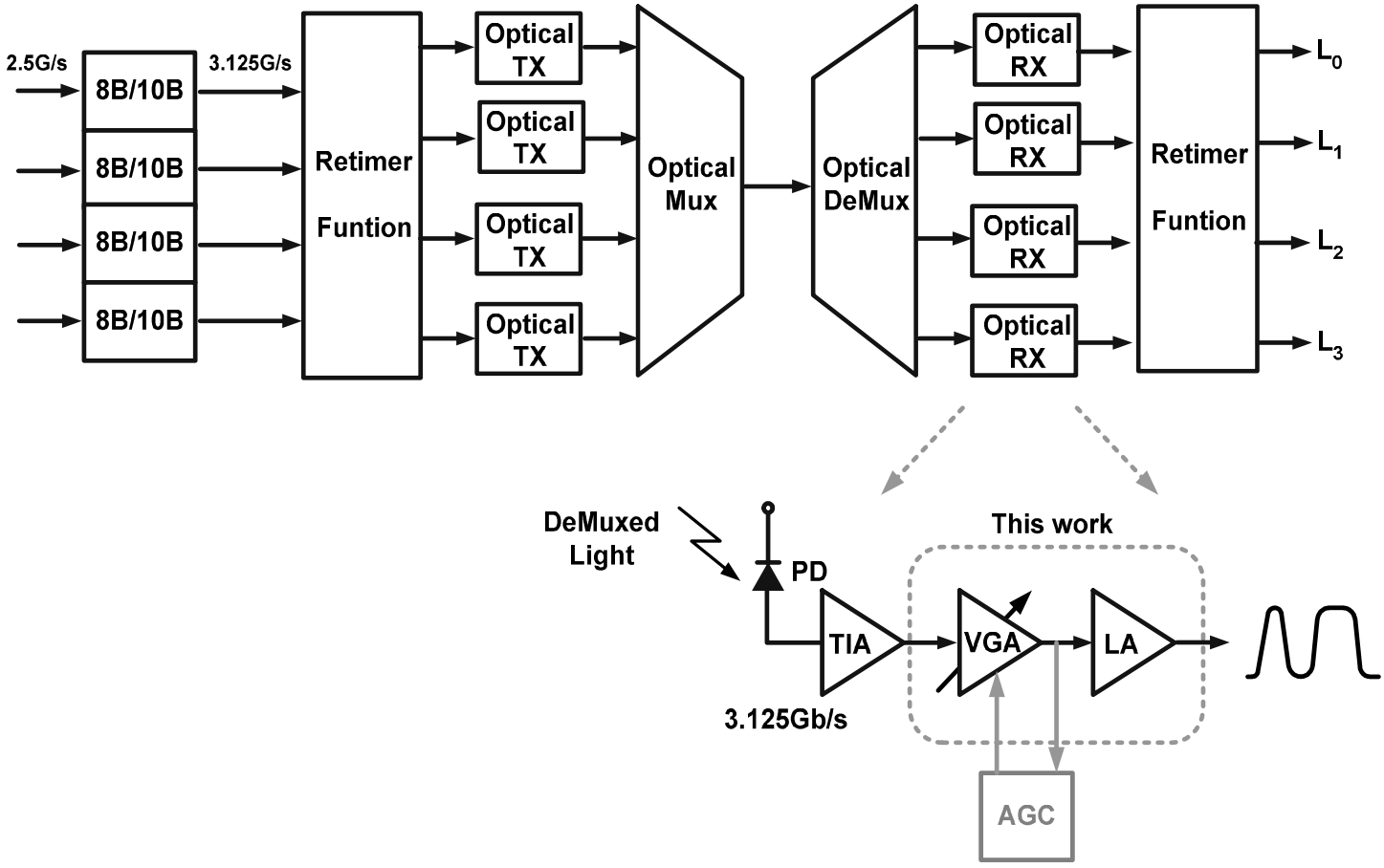
Technology	0.18μm CMOS
Gain Tuning Range	50dB (-16 dB ~ 34 dB)
Upper -3dB Bandwidth	2 GHz (± 5%)
Lower -3dB Bandwidth	400 kHz
S11 & S22 (midband)	< -10 dB
Sensitivity @ BER = 10^{-12}	9 mVp-p
AM to PM (8mV ~ 200mV)	< 20ps
Peak-to-Peak Jitter	< 95 ps
Power Dissipation @ with buffers	40 mW
Supply Voltage	1.8 V
Area	1.0 mm × 0.7 mm

Figure 26.8.7: Performance summary.



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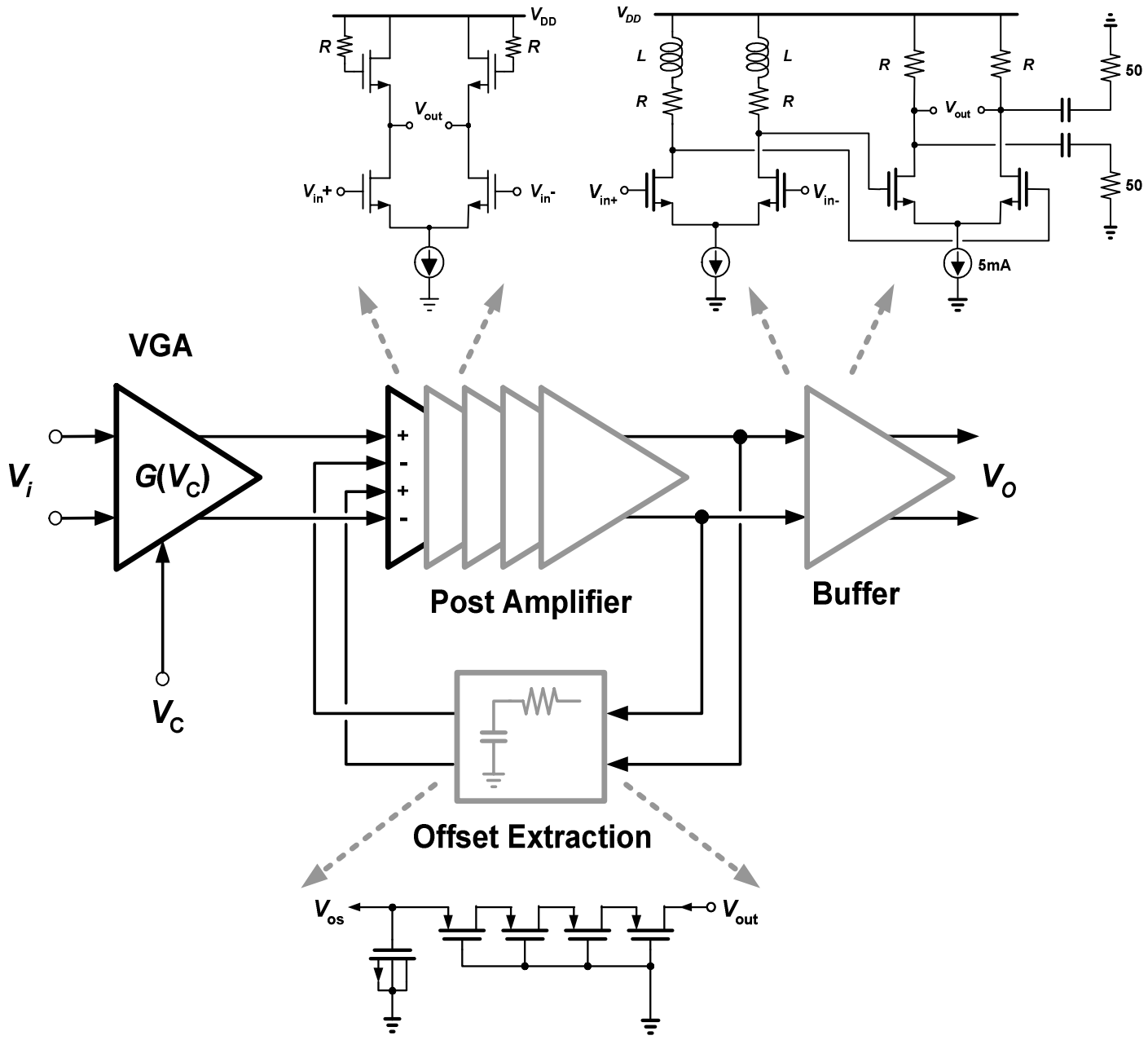

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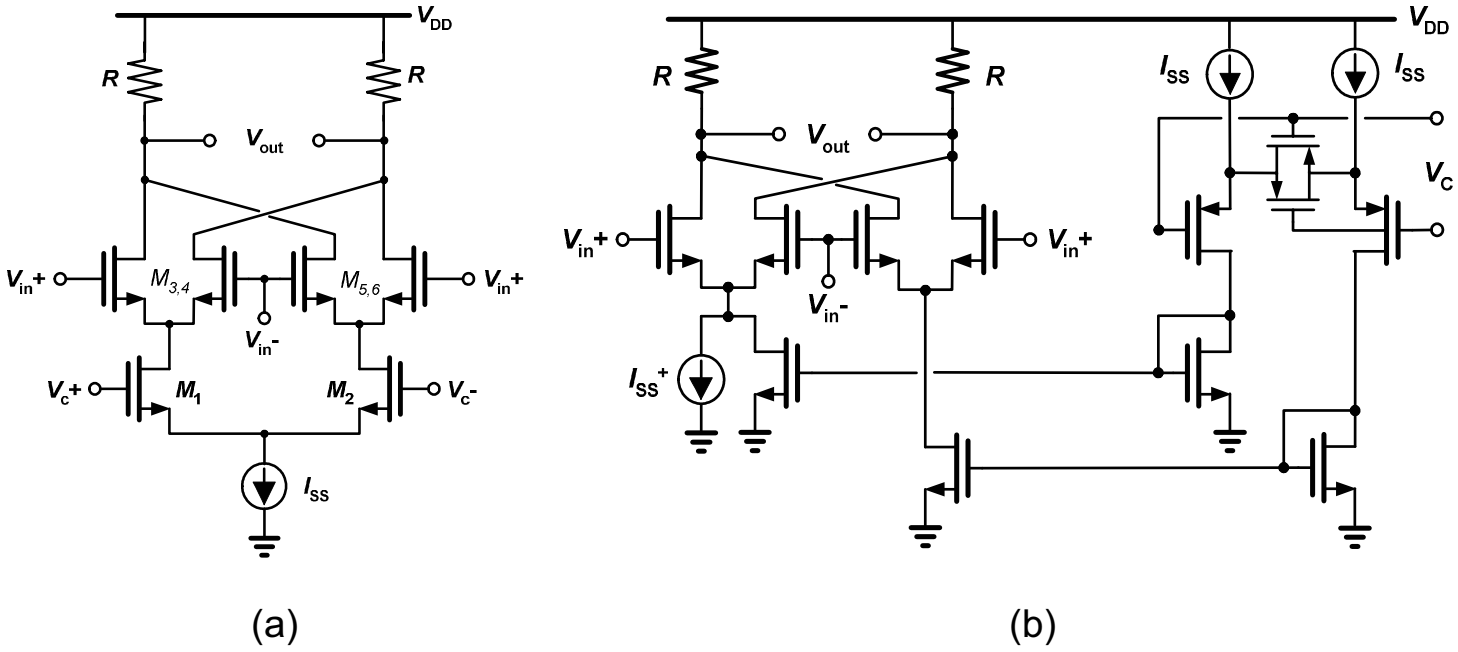

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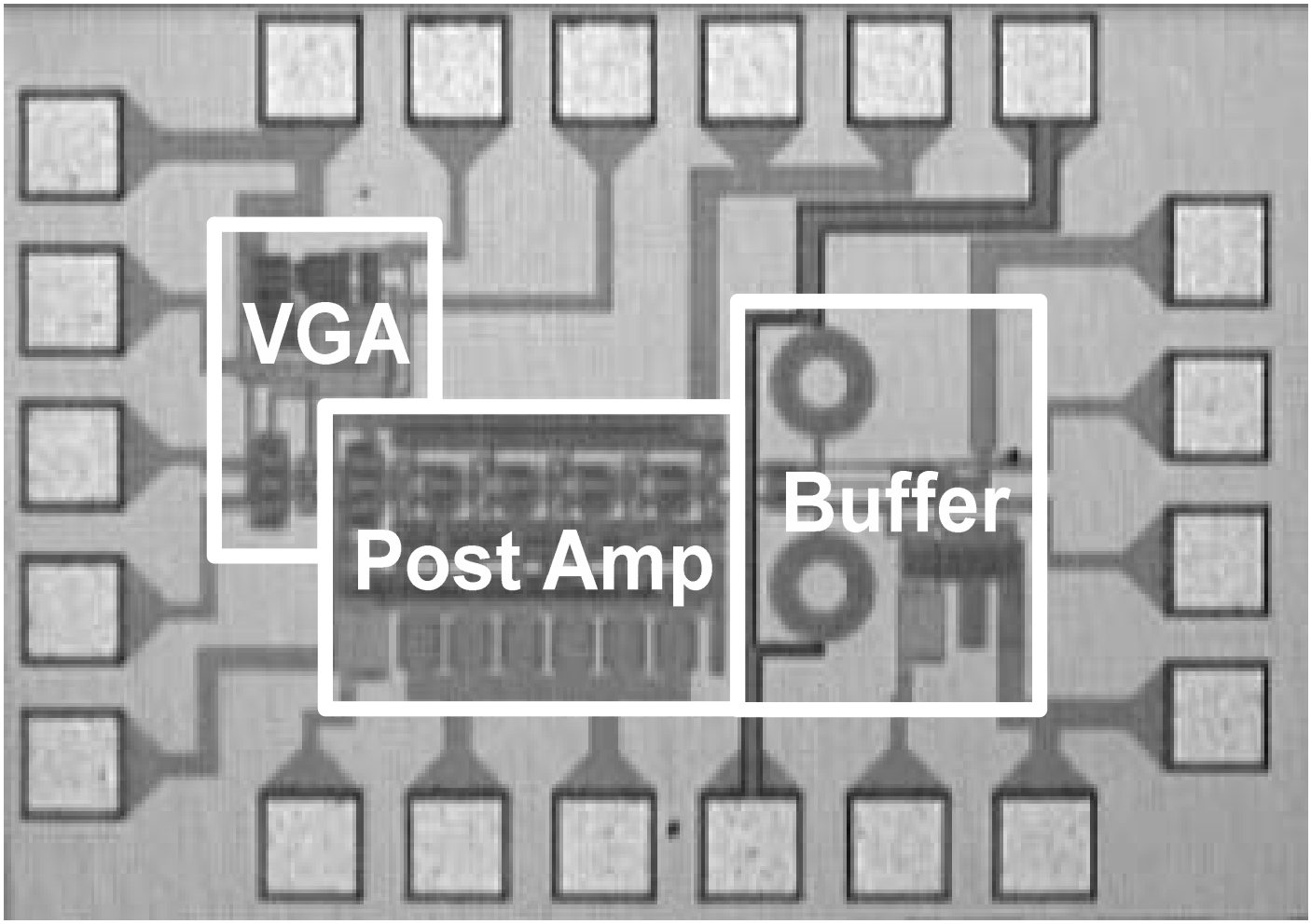

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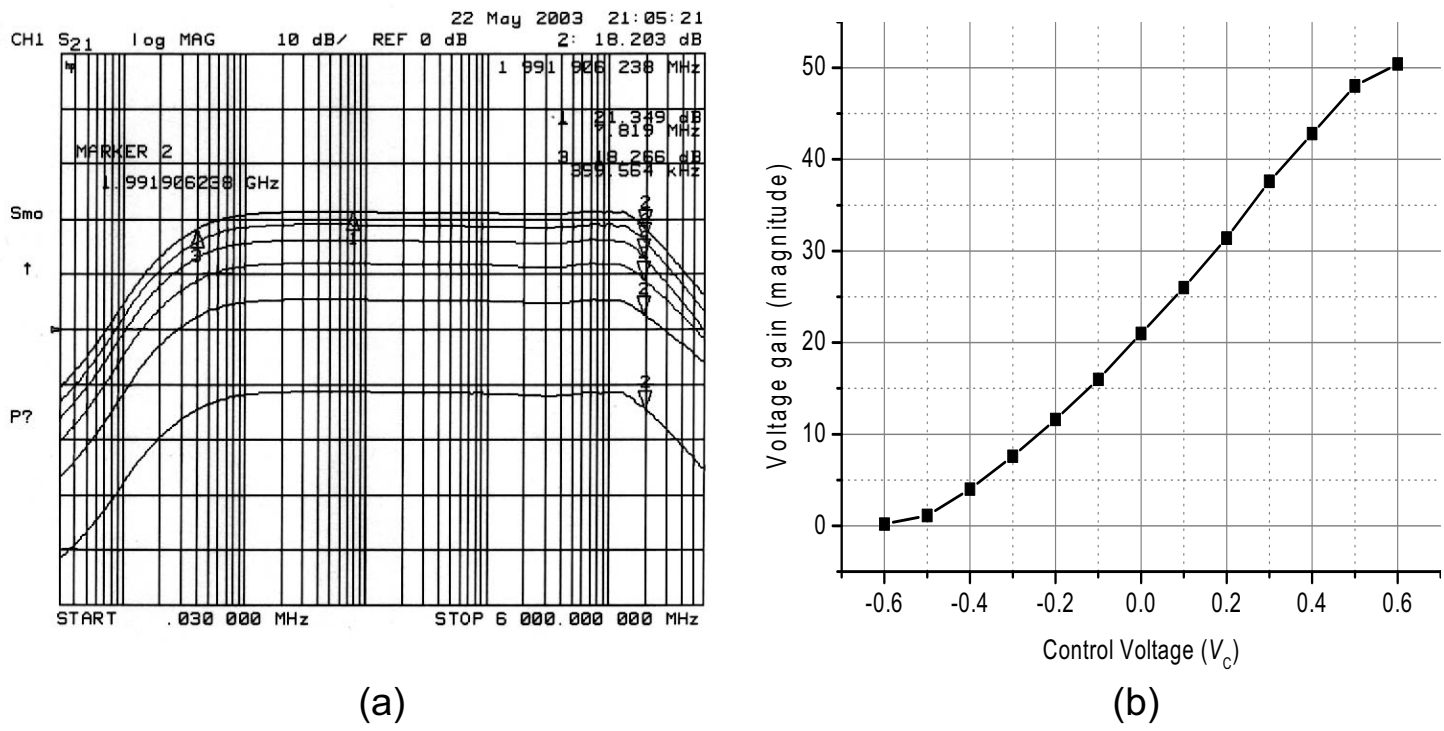

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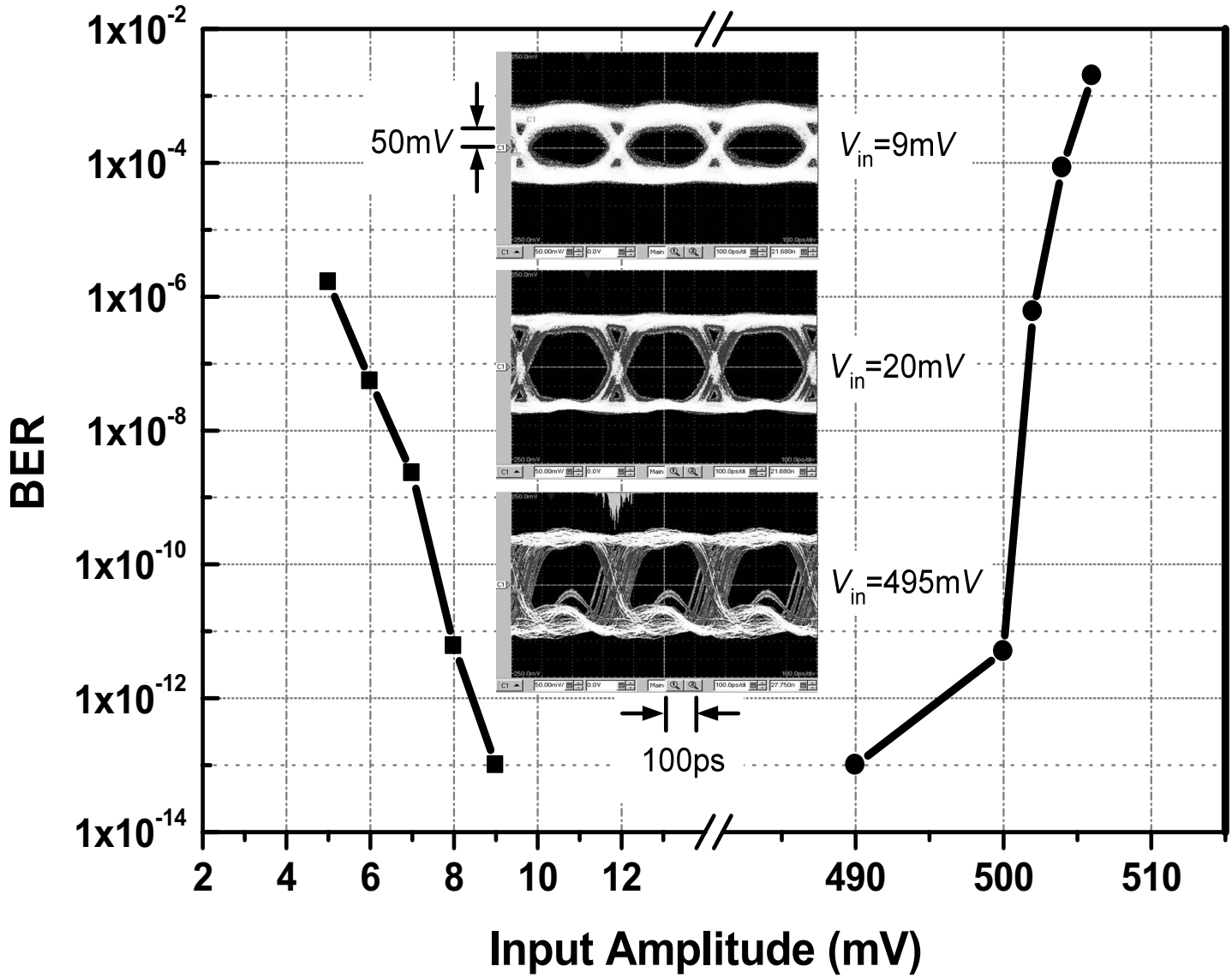

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