Chapter 5: A complex design case: the gain-boosted folded-cascode OTA.

We presented a first systematic study of the gain-boosted regulated-cascode OTA CMOS stage at the ESSCIRC'96 conference [Flandre '96b]. An extended study was then sollicited by the guest editors for publication in the Special issue of the IEEE Journal of Solid-State Circuits on ESSCIRC'96 [Flandre '97].

The gain-boosting technique has been proposed as a solution to the uneasy realization of folded-cascode CMOS operational amplifiers aiming both at large gain and large bandwidth performances [Bult '90, Bult '91]. It exploits the principle of the regulated-cascode stage [Hosticka '79] which is widely used in high-impedance current sources [Säckinger '90], current copiers [Goldenberg '94], etc … The problem actually is to design such a high-performance op. amp. without degrading its transient response. To our knowledge, only a partial solution based on an intuitive analysis was reported in [Bult '90, Bult '91].

Our work first exploits symbolic analysis techniques to get the complicated open-loop small-signal equations of the stage. The interest of the symbolic analysis lies in its ability to overcome the limitations of the usual intuitive analysis while keeping in the same time some physical insight into the complex pole-zero behavior.

One of the most important results of the study is that besides the pole-zero doublet mentioned in [Bult '90, Bult '91], the behaviour of a pair of complex conjugate poles also must be considered (Section 5.1). The generic symbolic closed-loop expression of the transfer function yields then a new design criterium aiming at the optimization of the settling time, rather than the phase margin (Section 5.2). A synthesis procedure based on the "gm/ID" methodology is considered furtheron for quick optimization of the architecture based the dc open-loop gain, transition frequency and settling time specifications (Section 5.3) and finally applied to practical design cases (Section 5.4).

5.1. Gain-boosted stage model.

A simplified small-signal schematic view of the basic gain-boosted folded-cascode CMOS stage is depicted in Figure 5.1. The main amplifier is the folded-cascode pair consisting of transistors M1 and M2. The purpose of the auxiliary stage M3 is to counteract the loss of gain which occurs inevitably when one attempts to widen the gain-bandwidth product of the main amplifier. Transistor M3 introduces a negative feedback loop which tends to make the source voltage of the common gate transistor M2 less sensitive to the output signal. Since the drain of the common source transistor M1 is better isolated from the output, the influence of the output signal upon the drain current is also lessened. The output impedance of the main cascode amplifier thus increases. This enhances the dc gain. It does not affect the transconductance of M1 however, thus the transition frequency remains the same.

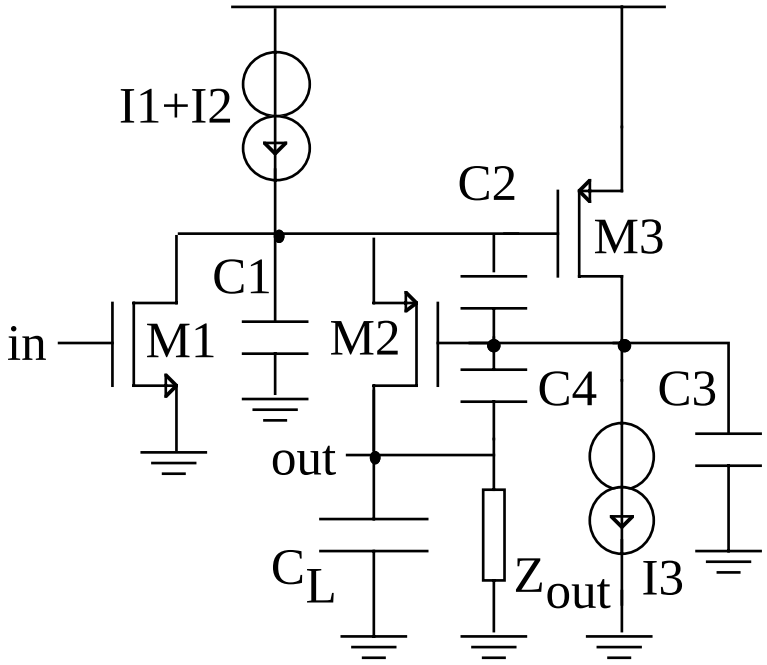

Figure 5.1: Simplified small-signal schematic view of basic gain-boosted folded-cascode OTA stage introducing notations.

The currents I1, I2 and I3 are the bias currents of M1, M2 and M3 respectively. All current sources are supposed ideal. The small-signal transconductances of M1, M2, M3 and their output conductances are noted g_{mi} and g_{di} respectively, with i = 1…3. Besides the capacitive load C_L, four parasitic capacitances are associated to the four nodes of the stage:

- C1 mainly corresponds to the parallel combination of the M1 drain-to-substrate, M2 source-to-substrate and M3 gate-to-source and gate-to-substrate capacitances;
- C2 to the M2 gate-to-source and M3 gate-to-drain capacitances;
- C3 to the M2 gate-to-substrate and M3 drain-to-substrate capacitances;

- C4 to the M2 gate-to-drain capacitance.

Their values are determined according to the expressions :

$$C1 = C_{jn}.W_1 + C_{jp}.W_2 + C_{gs3} + C_{gb3} \quad (5.1)$$

$$C2 = C_{gs2} + C_{gd3} \quad (5.2)$$

$$C3 = C_{gb3} + C_{jp}.W_3 \quad (5.3)$$

$$C4 = C_{gd2} \quad (5.4)$$

where W denotes the device width and C_{jn} and C_{jp} are respectively the n- and p-junction capacitances per unit of width (which include both bottom and sidewall components). C_{gs}, C_{gd} and C_{gb} are respectively the gate-to-source, -to-drain and -to-substrate device capacitances, which are functions of the inversion regime according to [Enz '95] but restricted here to their strong inversion classical approximations in saturation, i.e.

$$\begin{aligned} C_{gs} &\approx \tfrac{2}{3}.C_{ox}.W.L \\ C_{gd} &\approx C_{rec}.W \\ C_{gb} &\approx 0 \end{aligned} \quad (5.5),$$

with L the device length and C_{rec} the gate-diffusion overlap capacitance per unit of length. These simplifying approximations may result in some quantitative inaccuracy but do not induce any qualitative misinterpretation.

The use of the symbolic small-signal simulator ISAAC [Gielen '89] yields a quite complicated transfer function $A(s)=V_{out}/V_{in}$, with a third-order denominator and a second-order numerator, which are too lengthy to be usefully reproduced here. The dc open-loop gain A_0 assuming the active output load impedance Z_{out} is equal to the regulated-cascode stage output impedance is given by:

$$A_0 = -\frac{g_{m1}\cdot g_{m2}\cdot g_{m3}}{2.g_{d1}\cdot g_{d2}\cdot g_{d3}} \quad (5.6).$$

The actual gain boosting effect is illustrated by the multiplication of the gain of the main cascoded amplifier by the intrinsic gain of the auxiliary amplifier g_{m3}/g_{d3}.

To gain more insight into the small-signal behaviour of this amplifier, the frequency location of the poles and zeros as well as the open-loop transition frequency f_T and phase margin Φ_m of the stage were numerically evaluated considering a representative example. This was achieved by implementing the complete ISAAC solution in MATLAB. Therefrom we were able to analyze the influence of the auxiliary stage upon the movement of the poles and zeros of the op. amp. keeping M1 and M2 and their bias currents unchanged. In our example these were chosen equal to values typical of a folded-cascode design. The intrinsic gain of the auxiliary stage was also kept constant and chosen so as to boost the overall gain A_0 over a given value (100 dB here). Therefore, the ratio of the transconductance g_{m3} over drain current I3 remains

constant since g_{m3}/g_{d3} is also equal to $(g_m/I_D)_3.V_{ea3}$, V_{ea} being the Early voltage, a more or less constant value as long as the gate length of M3 remains the same.

This numerical approach of the open-loop transfer function behaviour is illustrated in figure 5.2 where the bias current of M3, plotted vertically, is the parameter under consideration. This is equivalent to analyzing the influence of g_{m3} or of the gain-bandwidth product of the auxiliary amplifier, GBW_3 equal to $g_{m3}/(C2+C3)$, as the ratio $(g_m/I_D)_3$ is fixed. This also means that the width of M3 is ajusted when I3 is changed and all parasitic capacitances are actualised in the same time. The evaluation of W_3 follows a pattern that will be described later under section 5.3. Figure 5.2.a shows that for low I3, a real pole-zero doublet is created below the transition frequency, in accordance with Bult's intuitive analysis [Bult '90, Bult '91]]. Increasing I3 repels this doublet to higher frequencies until it merges with the non-dominant pole of the main op. amp. to form a non-dominant complex conjugate pole pair which can be expressed as:

$$\mathrm{Re} \pm \mathrm{j}.\mathrm{Im} = \mathrm{Re}.\left(1 \pm \sqrt{\zeta^2 - 1}\right) \qquad (5.7),$$

where ζ is the damping factor equal to 1 in the case of a single real pole and smaller than 1 in the case of a pair of complex conjugate poles.

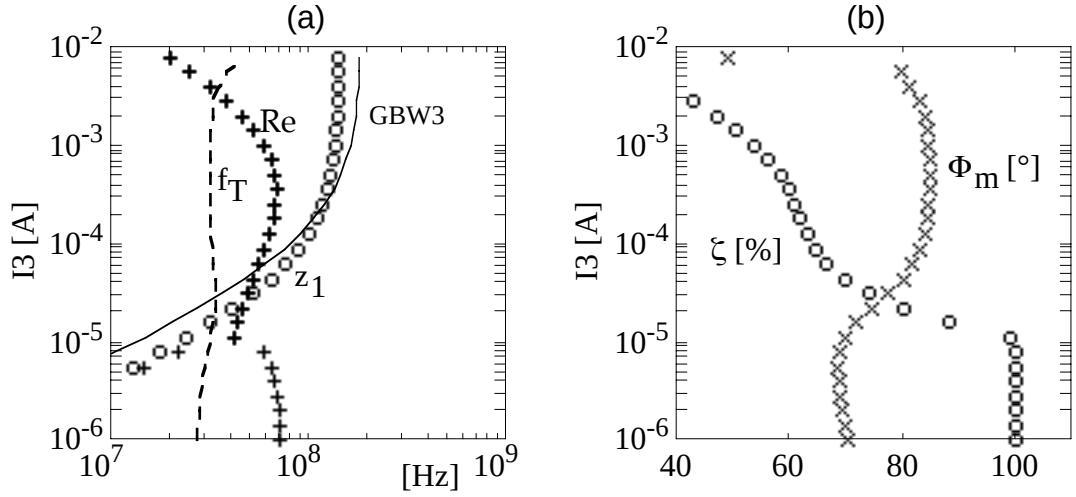

Figure 5.2 : Numerical transfer function analysis vs M3 bias current :
(a) non-dominant poles (+) , dominant zero (o), opamp transition frequency (- -) and M3 gain-bandwidth product (–), (the dominant pole and non-dominant zero are egal to 159 Hz and larger than 1 GHz resp. and are thus not shown);
(b) damping factor (o) and phase margin (x);
for C_L = 10 pF, g_{m1} = 1.9 mS, I_1 = 380 µA, g_{m2} = 1.5 mS, I_2 = 380 µA, $g_{m3}/I3$ = 4, $L_1 = L_2 = L_3$ = 2 µm and following 2 µm bulk CMOS technology parameters: n = 1.35, V_{ea} = 17 V, μ_n = 600 $cm^2/(V.s)$, μ_p = 250 $cm^2/(V.s)$, C_{ox} = 1.1 $fF/\mu m^2$, C_{jn} = 2.3 fF/µm, C_{jp} = 4.6 fF/µm, C_{rec} = 0.23 fF/µm.

Two open-loop frequency responses for low and high values of I3 and hence GBW_3, are compared in figure 5.3. No significant difference can be observed.

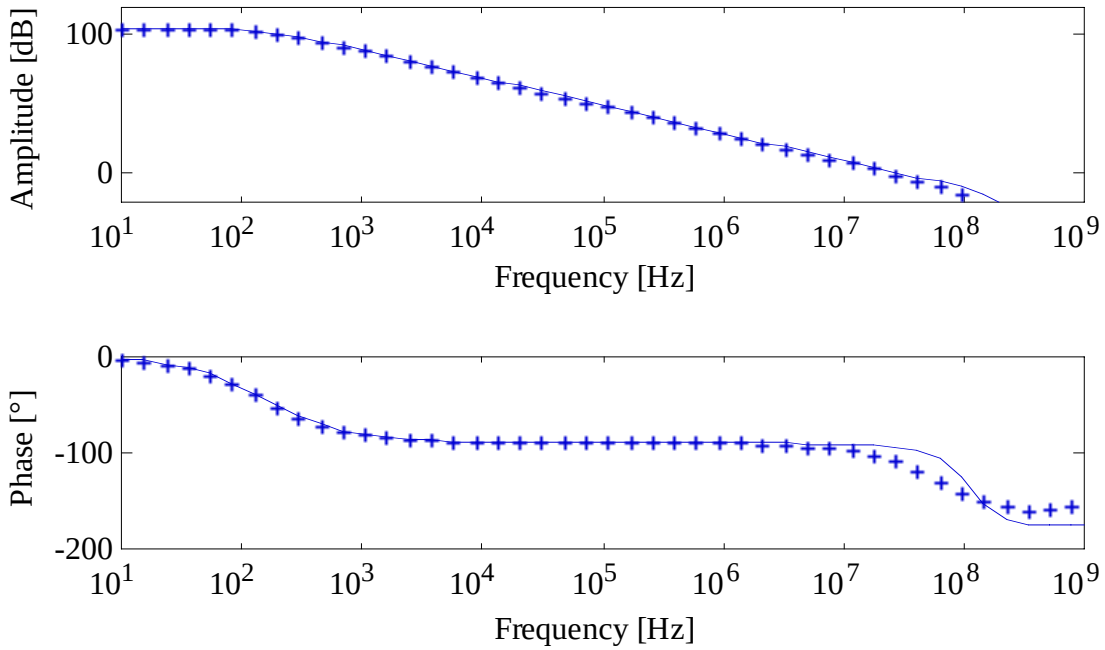

Figure 5.3: Bode diagrams of the open-loop transfer function with the parameters of figure 5.2 and I3 equal to 0.3 mA (–) or 5 µA (+).

The unity-gain closed-loop transient step response shows however substantial differences. This is illustrated in figure 5.4 which represents a set of curves of the step response error defined as $20.\log\{(V_{out}-V_{in})/V_{in}\}$, for various I3. Obviously after infinite time, all converge to a final error equal to $-20.\log(A_0)$. For low I3 and GBW_3 (Fig. 5.4.a), the low-frequency doublet predicted in [Bult '90, Bult '91] however results in an unacceptable slow settling component although the phase margin lies above the usual 60° margin commonly advocated for stabilization (Fig. 5.2.b). When I3 is increased according to Bult's intuitive design criterium which states that the gain-bandwidth product of the auxiliary stage (GBW_3) must lie somewhere between the closed-loop dominant and non-dominant poles, the slow settling component tends to disappear. This results in an acceptable although sub-optimal nominal settling time (Fig. 5.4.b) which however can be very sensitive to component mismatches and temperature variations since the acceptable design window is extremely limited (Fig. 5.2.a). In fact when GBW_3 is nearing the gain-bandwidth product of the main amplifier, the doublet is already overruled by the complex conjugate pole pair. For large I3, making the real part Re of this pole pair maximum, the step response finally shows a nice settling behavior (Fig. 5.4.c), almost as fast as that of an ideal first-order opamp with identical GBW and A_0 (Fig. 5.4.d). The corresponding phase margin is larger than 80° (Fig. 5.2.b). Still larger I3 however are unpractical since this lowers Re and degrades Φ_m as well as the settling time (Fig. 5.2).

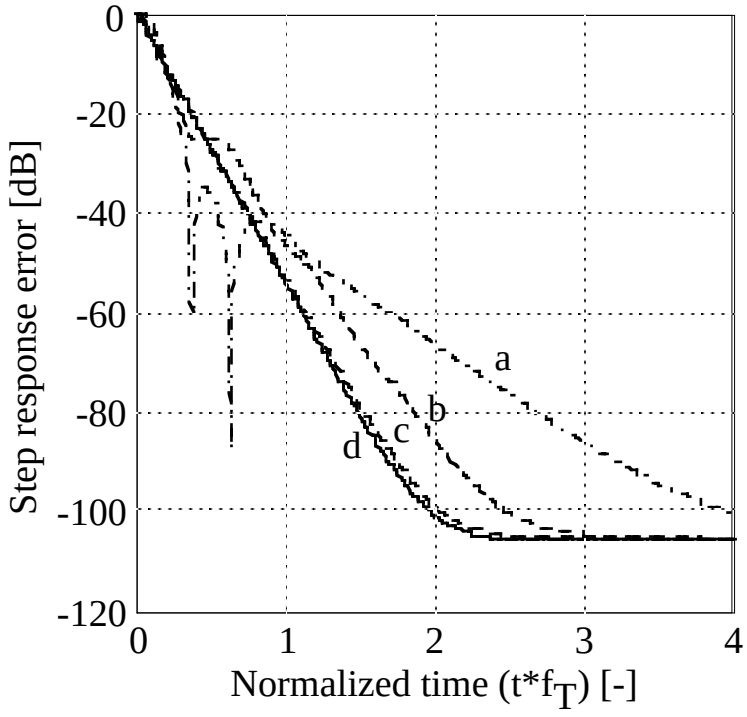

Figure 5.4: Closed-loop step time response error 20.log{(V_{out}-V_{in})/V_{in}} in various cases of figure 5.2: I3 = 5 µA (a), 30 µA (b), 0.3 mA (c) and first-order response with same A_0 and GBW (d).

5.2. Optimum design criteria.

In order to use these results for synthesizing opamps with specified performances, design criteria defining the optimal pole-zero positions are required, which suppose access to analytical relationships between the pole-zeros and the small-signal device parameters. The latter relationships were obtained from polynomial decomposition of the transfer function A(s) assuming that cases of practical interest always feature: 1) a complex conjugate pole pair instead of a doublet, 2) well separated poles and zeros, 3) the possibility to ignore the high-frequency zero, and 4) negligible transistor output conductances compared to the transconductances. Noting z_1 the first zero, A(s) can be expressed as follows :

$$A(s) = \frac{V_{out}}{V_{in}} \approx \frac{1}{\frac{1}{A_0} + \frac{s}{GBW}} \cdot \frac{1 + s / z_1}{1 + 2.\zeta^2 . \frac{s}{Re} + \zeta^2 . (\frac{s}{Re})^2} \qquad (5.8),$$

where z_1, Re, ζ, A_0, GBW and Φ_m are given in Table 5.I as functions of the small-signal device parameters. The close agreement between the analytical formulas and the previous numerical data is clearly demonstrated in figure 5.5 and underlines the power of symbolic analysis tools.

$$z_1 \approx \frac{-g_{m2}\cdot g_{m3}}{(C3+C4).g_{ms2}+C2.g_{mb2}-C4.g_{m3}} \qquad A_0 = -\frac{g_{m1}\cdot g_{m2}\cdot g_{m3}}{2.g_{d1}\cdot g_{d2}\cdot g_{d3}} \qquad GBW = \frac{g_{m1}}{C_L} \approx \omega_T = 2.\pi.f_T$$

$$Re \approx -\frac{(C3+C4).g_{ms2}+C_2.(g_{mb2}+g_{m3})}{2.\left(C2.(C1+C3+C4)+C1.(C3+C4)\right)} \qquad \Phi_m = 90° - a\tan\left(\frac{\omega_T+|Im|}{|Re|}\right) - a\tan\left(\frac{\omega_T-|Im|}{|Re|}\right) + a\tan\left(\frac{\omega_T}{|z_1|}\right)$$

$$\zeta \approx \frac{(C3+C4).g_{ms2}+C2.(g_{mb2}+g_{m3})}{\sqrt{4.g_{m2}\cdot g_{m3}.\left(C2.(C1+C3+C4)+C1.(C3+C4)\right)}} \qquad g_{ms2} = n.g_{m2} \qquad g_{mb2} = (n-1).g_{m2}$$

Table 5.I: Simplified analytical expressions of the transfer function characteristics as a function of the device transconductances g_m and output conductances g_d and of the node capacitances using the notations of Figure 5.1. (*n* corresponds to the linearized MOS body effect parameter, g_{ms} and g_{mb} to the source and body transconductances according to the EKV model [Enz '95]).

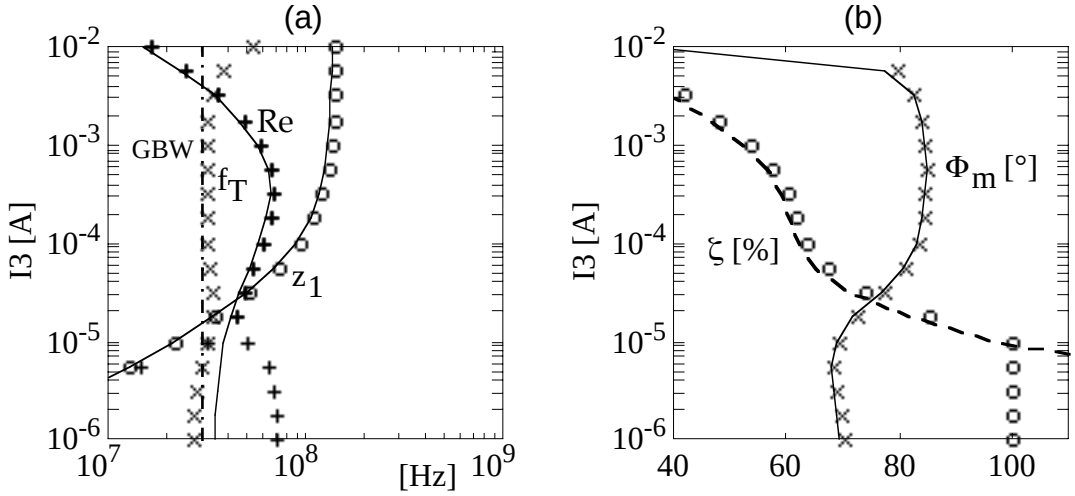

Figure 5.5: Comparison of the numerical (symbols) and analytical (lines) transfer function analyses vs M3 bias current, in the same conditions as in figure 5.2:
(a) non-dominant poles (+) , dominant zero (o), opamp gain-bandwidth product (— · —) and transition frequency (x);
(b) damping factor (o) and phase margin (x);
the analytical approximations for Re and ζ are obviously only valid in the case of a complex conjugate pole pair.

Since phase margin optimization is not sufficient to ensure fast settling, our prime objective was to work out criteria which optimize the settling time towards that of the ideal first-order opamp with the same gain A_0 and gain-bandwidth product GBW. To determine the required pole-zero locations we investigated the generic unity-gain closed-loop step function response of the opamp transfer function A(Ω) normalized to f_T, i.e. $\Omega = s/(2.\pi.f_T)$, $nz = z_1/(2.\pi.f_T)$ and $np = Re/(2.\pi.f_T)$. We defined the settling time as the time required to achieve a step response log error very closely nearing the A_0 specification, here first arbitrarily taken equal to $-20.\log(A_0)$ + 1 dB.

We computed the corresponding np-nz-ζ locus for correct settling, separating the design space into two regions, i.e. acceptable or not (Fig. 5.6). A good compromise is achieved when ζ ≈ 0.75, np ≈ 1.4 and nz ≈ 1.7, because for smaller or larger ζ, either the zero or the pole should be repeled respectively to higher frequencies, which may prove uneasy in practical opamp designs.

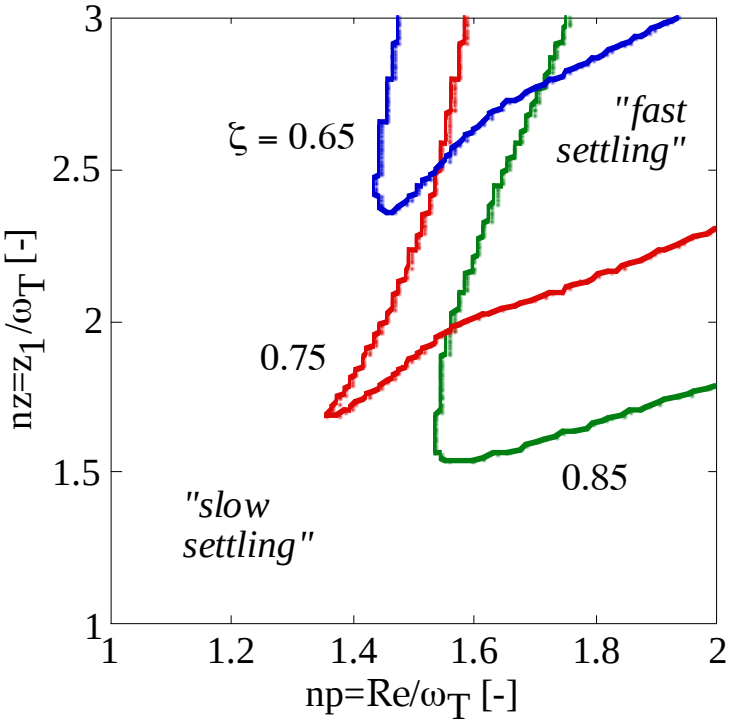

Figure 5.6: Pole-zero loci and design spaces (refered to f_T) for various fixed damping factor ζ and correct settling time performance egal to (-20.log(A_0)+1) dB.

An intuitive explanation of this is provided by the examination of the closed-loop response. From (5.8), the closed-loop transfer function

$$H(\Omega) = \frac{A(\Omega)}{1 + A(\Omega)} \qquad (5.9),$$

can generically be written as:

$$H(\Omega) = \frac{1}{1 + \frac{1}{A_0} + \frac{\Omega}{dp©}} \cdot \frac{1 + \Omega / nz}{1 + 2.\xi^2 . \frac{\Omega}{ndp©} + \xi^2 . (\frac{\Omega}{ndp©})^2} \qquad (5.10),$$

where dp', ndp' and ξ denote the closed-loop real pole and complex conjugate pole pair real part and damping factor respectively. After identification of (5.8), (5.9) and (5.10) and taking into consideration the fact that A_0 is large obviously, we have

$$np = ndp' + \frac{dp'}{2}$$

$$\zeta^2 = \left(ndp' + \frac{dp'}{2}\right).\left(\frac{\xi^2}{dp'.ndp'} + \frac{\xi^2}{2.ndp'^2}\right) \qquad (5.11),$$

$$nz = \left(\frac{1}{dp'} + \frac{2.\xi^2}{ndp'} - 1\right)^{-1}$$

and the step time response is:

$$y(t) \approx a_1 + a_2.e^{-dp'.t} + e^{-ndp'.t}.\left(a_3.e^{j.Im'.t} + a_4.e^{-j.Im'.t}\right) \qquad (5.12),$$

with $Im' = \left|ndp'\sqrt{1-\xi^2}\right|$.

From (5.12), it is now clear that the optimization of the closed-loop step time response requires both dp' and ndp' to be close to 1, to avoid any slow component, and ξ to be of the order of 0.5 to provide just sufficient amount of damping, which from (5.11) yields np ≈ 1.5, nz ≈ 2 and ζ ≈ 0.75 in open loop. This does not only validate the optimum design criterium discussed previously, but also generalizes the optimization criterium of such generic third-order stage time response, independently from any particular condition, e.g. a step response log error criterium arbitrarily different from (-20.log(A_0)+1) dB.

5.3. Systematic design methodology.

We now propose a design procedure based on the above results which follows the "gm/ID" design methodology for CMOS OTAs described previously, e.g in [Silveira '96]. The approach will be illustrated by means of an example targeting a gain A_0 of 90 dB and a transition frequency f_T of 100 MHz, considering a load C_L equal to 10 pF in a 2 µm-bulk CMOS technology whose parameters were given in Figure 5.2.

a) The design starts with the sizing of the folded-cascode stage M1-M2 for the specified transition frequency f_T and phase margin (i.e. $\Phi_m \approx 60°$) assuming I1 is equal to I2. The outcome is a relatively low gain device. A simple two-pole behavioral model of this stage is sufficient to provide an adequate initial guess for the regulated-cascode design which follows later. The sizing of M1 and M2 is based on the "gm/ID" methodology which proceeds along the lines described in figure 5.7 and is explained hereafter.

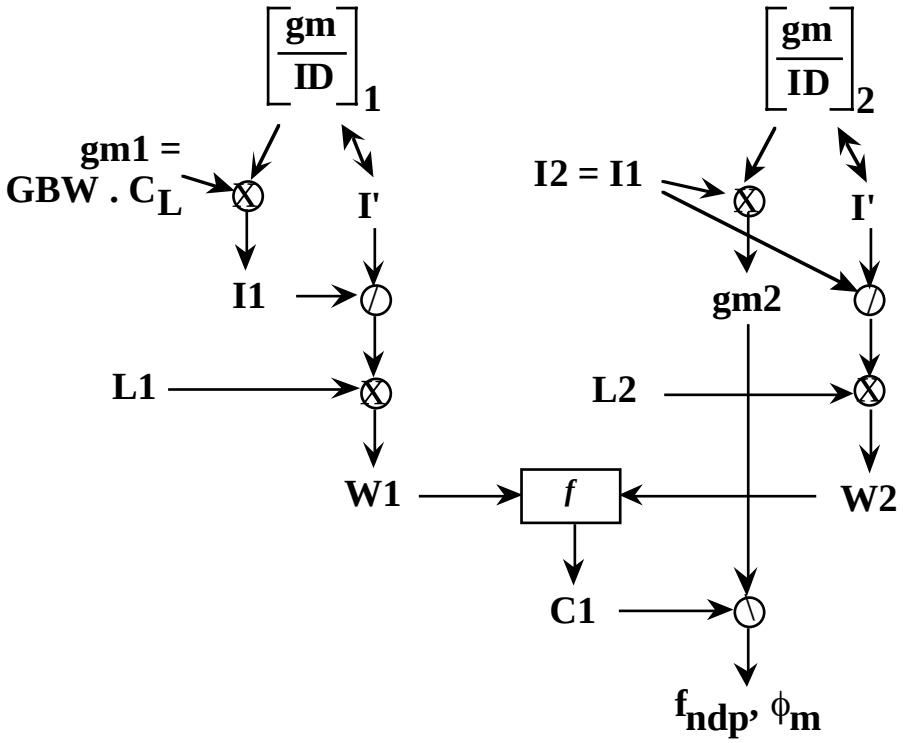

Figure 5.7: Design flow for the folded-cascode stage M1-M2
implementing the "gm/ID" methodology.

1° Starting from the known gain-bandwidth specification we first evaluate the required transconductance g_{m1}. A set of drain currents I1 is then infered from a set of realistically chosen (g_m/I_D) ratios for M1. Since the latter are size-independent, the EKV model [Enz '95] unambiguously yields the scaled drain currents $I' = I_D/(W/L)$, W/L being the aspect ratio. The actual W/L ratios are found from the ratios of drain currents over scaled drain currents. Therefrom we determine the set of W_1's given a minimal channel length L_1 for such high-frequency specifications.

2° The position of the folded-cascode non-dominant pole given by $f_{ndp} = n.g_{m2}/C1$ (where C1 is obtained from (5.2) and (5.6) setting $W_3 = 0$) is then computed for each (g_m/I_D) possible choice for M2. Each time, I' is derived from the EKV model and W_2 found from I2/I' with $L_2 = L_1$ and I2 = I1. The latter condition also yields g_{m2} for each $(g_m/I_D)_2$, so that the non-dominant pole can be calculated from g_{m2}, W_1 and W_2, and compared to f_T.

Figure 5.8 graphically presents the result of this algorithm versus $(g_m/I_D)_1$. The limits of the acceptable design window correspond to a non-dominant pole lying at 1.73 times f_T for $\Phi_m = 60°$. We then note that for a given choice of $(g_m/I_D)_1$, there may be either two, or one, or zero solutions to the folded-cascode design problem for the specified conditions. This can be clarified considering the strong inversion approximation of the transconductances. Setting

$$f_{ndp} = n.g_{m2}/C_1 = 1.73\ \omega_T = 1.73\ g_{m1}/C_L,$$

the relation:

$$\frac{1}{C_{jn}.W_1 + C_{jp}.W_2}.\sqrt{n.2.\mu_p.C_{ox}.\left(\frac{W}{L}\right)_2.I2} = \frac{1.73}{C_L}.\sqrt{\frac{2.\mu_n.C_{ox}}{n}.\left(\frac{W}{L}\right)_1.I1} \qquad (5.13),$$

imposes, for given values of $(g_m/I_D)1$, W_1, $L_1 = L_2$ and I1 = I2, a constraint on W_2 which may be expressed by means of a quadratic equation of the form

$$a.W_2^2 + b.W_2 + c.W_1^2 = C_{jp}^2.W_2^2 + \left(2.C_{jn}.C_{jp}.W_1 - \frac{k}{W_1}\right).W_2 + C_{jn}^2.W_1^2 = 0 \qquad (5.14),$$

where k corresponds to the ratio of the technological parameters in (5.13). Depending on W_1, the determinant of equation (5.14) can be either positive, zero or negative and result in either two, one or zero real positive solutions for W_2. The determinant will only be positive if W_1 is smaller than a given constraint. Intuitively, a too large choice of $(g_m/I_D)1$ may result in an already too large value for C1 so that no choice of $(g_m/I_D)2$ will be able to repel the non-dominant pole towards an acceptable position.

We chosed $(g_m/I_D)1 = 5$ and $(g_m/I_D)2 = 3$ as a convenient starting point, representing a reasonable compromise between gain (i.e. 66 dB) and power consumption.

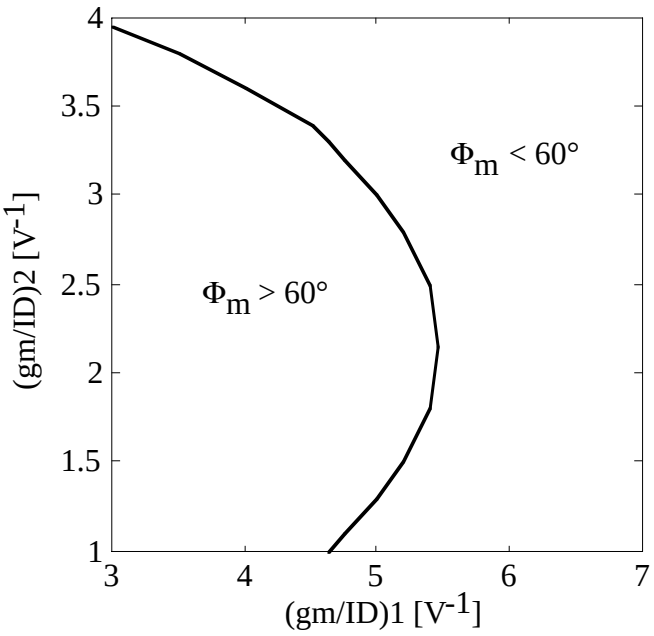

Figure 5.8 : Design space for folded-cascode M1-M2 stage with GBW = 100 MHz and technological data of figure 5.2.

b) The auxiliary amplifier with the required gain is then added and I3 raised until entering the acceptable np-nz-ζ design space. If this proves impossible, the equations of Table 5.I are used to properly adapt the design of M1 and M2. In our example, a $(g_m/I_D)_3$ close to 1 is sufficient to achieve the targeted A_0. The associated pole-zero analysis shown in figure 5.9 indicates however that both np and ζ remain much too low so that fast settling cannot be achieved, eventhough the design solution proposed in [Bult '90, Bult '91] can be met, i.e. placing GBW_3 close to f_T. From the equations of Table 5.I, we see that in order to raise both np and ζ, the ratio $g_{m2}/(C1.C2)$ must be increased. This implies increasing I2 to raise g_{m2}, while decreasing the (g_m/I_D) ratios of M1 and M2 to limit their widths and associated capacitances and increasing the (g_m/I_D) of M3 to maintain A_0. The procedure eventually leads, for $(g_m/I_D)_1$ = 2, $(g_m/I_D)_2$ = 2.8 and $(g_m/I_D)_3$ = 2.75, to an acceptable solution in terms of settling considering I3 = 6 mA (Fig. 5.10). Table 5.II details the result of the optimization.

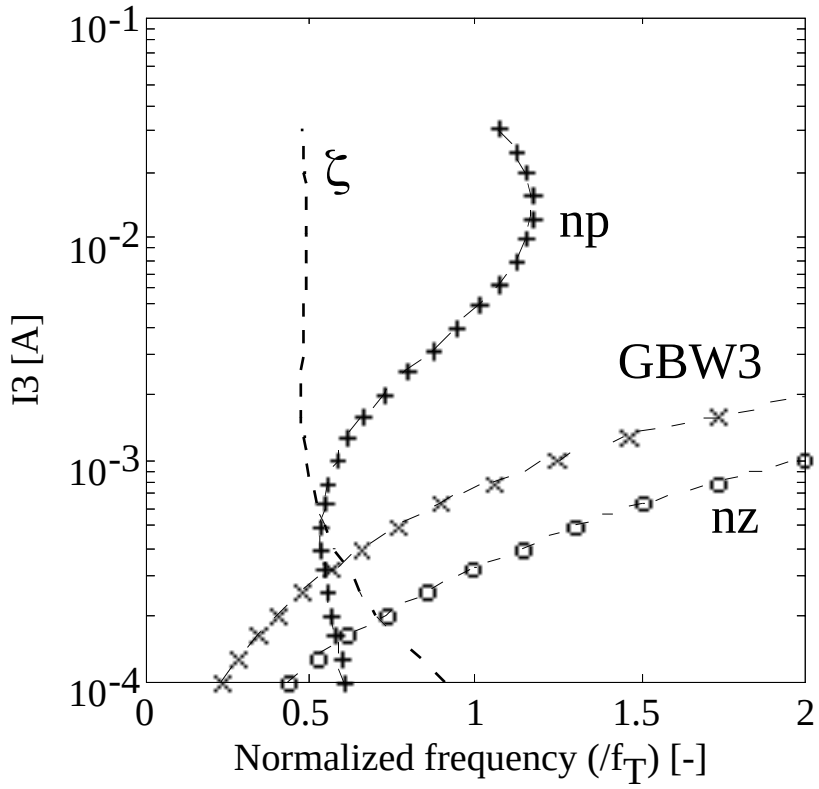

Figure 5.9: Pole-zero analysis (refered to transition frequency) vs M3 bias current: np (+), ζ (- - -), nz (o), GBW_3 (x) for g_{m1} = 6.5 mS, g_{m2} = 3.9 mS, I1 = I2 = 1.3 mA, $(g_m/I_D)_3$ = 1 and other parameters as in Fig. 5.2.

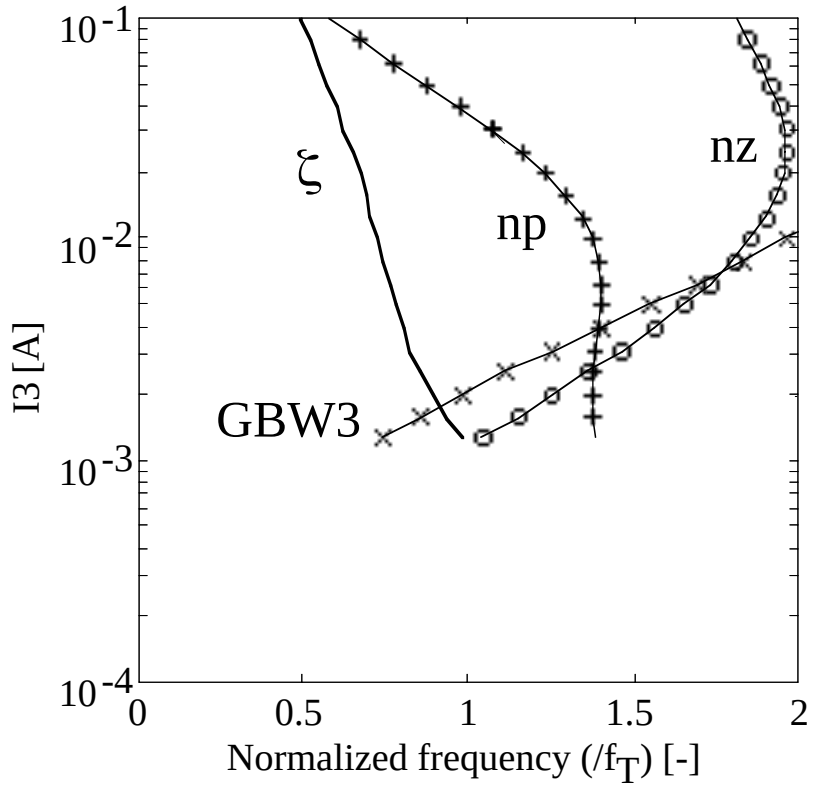

Figure 5.10: Pole-zero analysis (refered to transition frequency) vs M3 bias current: np (+), ζ (–), nz (o), GBW_3 (x) for g_{m1} = 6.2 mS, g_{m2} = 35 mS, I1 = 3.1 mA, I2 = 12.6 mA, $(g_m/I_D)_3$ = 2.75 and other parameters as in Fig. 5.2.

5.4. Discussion

The very large device sizes and small output swing - estimated, from the (g_m/I_D) ratios, to be much less than 1V under 5 V supply voltage - however indicate that the solution we reached for 90 dB - 100 MHz specifications is too close from the limits of a 2 µm bulk CMOS technology as used in [Bult '90, Bult '91] (Table 5.II.a). To get a more practical solution, either lower target performances or more performing technology should be chosen. The first option can be illustrated by the design case we used in sections 5.1 and 5.2 to support our analysis, which was indeed already treated following the guidelines of our systematic design methodology. The results are reproduced in Table 5.II.b for sake of comparison. The second option is illustrated by a 90 dB - 100 MHz target design in a 2 µm thin-film SOI CMOS technology which presents well-known analog advantages [Flandre '96a], i.e. low body effect and drain parasitic capacitance parameters as shown in Table 5.II. The SOI design solution outperforms the bulk result in terms of die area and stand-by current for even slightly superior gain, transition frequency and settling performances (Table 5.II.c). An actual 2-µm SOI implementation indeed achieved 115 dB-A_0 and 115 MHz-f_T with a load of 10 pF at room temperature and even satisfactory operation up to 400°C [Gentinne '97].

The 90 dB - 100 MHz bulk CMOS example nevertheless demonstrate that our design methodology may also converge towards solutions nearing the technology limits, in which intuitive or SPICE-based approaches would generally fail. Furthermore it is worth to point out that all the MATLAB calculations related to the synthesis procedure are achieved in short CPU times, on the order of minutes, so that they may be repeated a large number of times searching for the optimal design space or incorporating other specifications, e.g. the minimization of power consumption.

	(a) Bulk	(b) Bulk	(c) SOI
(W/L)1 (µm)	246/2	184/2	500/2
(W/L)2 (µm)	4505/2	283/2	553/2
(W/L)3 (µm)	2131/2	225/2	23/2
I1 (mA)	3.1	0.38	1.3
I2 (mA)	12.6	0.38	1.3
I3 (mA)	6	0.3	0.14
A0 (dB)	89	105	96
fT (MHz)	94	31	107

Table 5.II: Optimization results of systematic design methodology for gain-boosted regulated-cascode CMOS stages:
(a) with dc open-loop gain and transition frequency performances close to 90 dB and 100 MHz on 10 pF-load, using the 2 µm-bulk CMOS technology parameters given in figure 5.2,
(b) with dc open-loop gain and transition frequency performances close to 100 dB and 30 MHz on 10 pF-load, using same technology parameters as in case (a),
(c) with dc open-loop gain and transition frequency performances close to 90 dB and 100 MHz on 10 pF-load, using the 2 µm-SOI CMOS technology following parameters: n = 1.1, V_{ea} = 17 V, μ_n = 600 $cm^2/(V.s)$, μ_p = 250 $cm^2/(V.s)$, C_{ox} = 1.1 $fF/\mu m^2$, C_{jn} = 0.58 fF/µm, C_{jp} = 0.64 fF/µm, C_{rec} = 0.23 fF/µm.

5.5. Conclusion

A systematic study of the basic gain-boosted regulated-cascode OTA CMOS stage has been reported, illustrating the benefits of combining symbolic analysis and "gm/ID" methodology. Our design approach not only showed the limitations of the intuitive analysis presented in [Bult '90, Bult '91] but yielded also design equations, criteria and procedures missing in the previous approach. The symbolic analysis was able to point out the occurence of a complex conjuguate pole pair in practical cases and lead to a general formulation of the design space for correct settling optimization. Furthermore a "gm/ID"-based synthesis of both the folded-cascode and gain-boosted regulated-cascode stages has been proposed for rapid optimization of the architecture towards dc open-loop gain, transition frequency and settling time specifications. The efficiency and advantages of the technique have been discussed in practical design cases.

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