SDR Forum Workshop on Rapid FPGA Development for Wireless Applications – IP Cores, Tools, and Standards

17 September 2009 • San Jose, California

This workshop will arm communications systems engineers, application developers and other technologists with the knowledge they need to implement software defined and cognitive radio systems utilizing FPGA based processing, and allow them to work with leading experts in FPGA design processes and tools to reduce the time and cost associated with FPGA development. The workshop will begin with an introductory keynote from Xilinx, followed by presentations by leading IP and application developers for FPGAs. The morning session will conclude with a panel discussion on exploring design requirements for FPGAs. The afternoon session will begin with presentations from leading tool and technology vendors supporting the development of FPGA based applications, to be followed by presentations from organizations promoting specifications also supporting FPGA based application development. The workshop will then conclude with a panel session exploring next steps in the evolution of FPGA development.

Workshop Agenda

7:30 to 8:30	**Breakfast and Registration**
8:30 to 8:40	Welcome and Introduction – John Chapin, Chair of *The SDR Forum*
8:40 to 9:20	Keynote Address, "The Fastest, Most Cost Effective Way from Development to Production: FPGA or ASSP?" presented by Manuel Uhm, Director of Wireless Communications, *Xilinx*
9:20 to 9:45	"SDR Waveform development techniques for FPGA," presented by Chandrasekar Raj of *ViaSAT*
9:45 to 10:10	"Challenge and solution for high performance IF-Over-PCI system," presented by Frederic Pirot of *R-Interface*
10:10 to 10:30	**Coffee Break**
10:30 to 10:55	"Automatic Synthesis of Flexible Multiprocessor Systems from Parallel Programs," presented by Harold Ishebabi of *Spectrum Signal Processing by Vecima*
10:55 to 11:20	"An Open Source FPGA Infrastructure for Heterogeneous Component-Based Systems," by Jim Kulp of *Mercury Federal Systems* and Shep Siegel, of *Atomic Rules, LLC*
11:20 to 11:45	"Hosting High Assurance Cryptographic architectures in an FPGA," by John Andolina of *ViaSAT*
11:45 to 12:15	"Processors for Digital Signal Processing: A Changing Landscape" by Jeff Bier, President, *BDTI*
12:15 to 1:30	**Networking Lunch and Demos**
1:30 to 1:55	"Using MATLAB and Simulink for the Design and Early Verification of Wireless Systems," presented by John Irza of *the Mathworks*
1:55 to 2:20	"Architecturally Optimized IP and High Level Synthesis for Rapid Algorithm Implementation and Verification in FPGA and ASIC technologies," presented by Doug Johnson of *Synopsis*
2:20 to 2:45	"Next-Generation FPGA Middleware - Minimizing Latency in Multi-Processing SCA-Compliant Platforms," presented by Steve Jennis of *PrismTech*
2:45 to 3:00	**Coffee Break**
3:00 to 3:30	"MHAL for FPGA," presented by Don Stephens of the *JTRS JPEO*
3:30 to 4:00	"OCP Corporate Introduction," presented by Ian Mackintosh, President and Chairman of *Open Core Protocol International Partnership (OCP-IP)*
4:00 to 5:00	Panel session and roundtable discussion on closing the gap between FPGA developers and tools

More information at www.sdrforum.org

Presentation Details

8:40 to 9:20

Keynote Address, “The Fastest, Most Cost Effective Way from Development to Production: FPGA or ASSP?” presented by Manuel Uhm, Director of Wireless Communications, *Xilinx*

Abstract: FPGAs have continued to enable the maturity of SDR technology from defense to commercial wireless infrastructure. In particular, the increased development cost of semiconductors has favored FPGAs over ASICs and ASSPs in production to address medium-sized markets such as wireless infrastructure. In addition, standards such as CPRI, OBSAI and SRIO for connectivity, and 3GPP and WiMAX for air interface protocols, enable interoperability and foster the development of IP and a supporting ecosystem to enable rapid development and faster time-to-market. This presentation will provide an overview of how FPGAs are enabling SDR to be first-to-market but also at lower BOM costs, including a competitive analysis vs. ASSPs.

About the Speaker: Manuel Uhm is the Director of Wireless Communications for Xilinx. Uhm is responsible for managing the commercial wireless
an ex
and Chair of the Markets Committee of the SDR (Software Defined Radio) Forum, as well as being on the Advisory Board for PennWell’s Military & Aerospace Electronics Forum.

Uhm joined Xilinx in 2004 and is a thought leader in identifying trends in software defined radio, digital signal processing, and other c
Electronic Business, Wireless Systems Design, Portable Design, COTS Journal, Military Embedded Systems, and Military & Aerospace Electronics, as well as having spoken at a number of conferences and industry events, such as the LTE World Summit, Wireless China, SDR Forum Technical Conferences and Workshops, IDGA Software Radio Summit, IQPC SDR Europe, the Military Technologies Conference and the Military Radios Conference.

Prior to joining Xilinx, Uhm worked at Spectrum Signal Processing, Inc., a leader in Software Defined Radio subsystems, where he was responsible for the Marketing Department.

Uhm received his master of business administration from Simon Fraser University and studied electrical engineering at Queen’s University.

9:20 to 9:45

“SDR Waveform development techniques for FPGA,” presented by Chandrasekar Raj of *ViaSAT*

Abstract: Software defined radio (SDR) technology utilizes reconfigurable hardware platforms to support multiple waveforms and standards. The latest FPGA architectures provide massive amounts of digital logic, RAM, and DSP resources along with flexible, high-speed, data interfaces. These resources make FPGAs an attractive solution for SDRs running at high bit rates, 300Mbps or more. Some waveforms have high enough bit rates or complexity to require the resources of multiple FPGAs. When this occurs, a WLP (Waveform Logic Part
One WLP technique is to break the waveform down into modular components (FFT, Filter, CORDIC, etc.) and design RTL modules for each component. Common programming and data interfaces are defined for all components making it easier to build components back into a full waveform. Care must be taken to design FPIM (FPGA Platform Independent Modules) to allow for ease in porting and reusability. ViaSat design
Effective WLP design for FPGAs and general principles for efficient waveform design will be discussed along with techniques for power savings in FPGA based designs.

About the Speaker: Chandrasekar Raj is the Program Manager of ASIC & IP Strategic Business Unit for ViaSat. Raj is responsible for managing and marketing commercial ASIC business and IP products that include Digital Video Broadcast and Forward Error Correction IPs. He has over 13 years of experience in semiconductor design, strategic marketing and business management. Raj joined ViaSat/ECC in 2002 and was instrumental in setting up ASIC infrastructure. He managed design verification for successful IpSTAR and SkyPHY ASICs. Prior to joining ViaSat, Raj consulted for NEC, Toshiba and was involved in Rx5900, Tx7901, Vr5432 and Vrc5477 MIPS processor design & verification. Raj received his MBA in marketing from Case Western Reserve University and M.Eng in wireless communication & signal processing from University of Illinois. He is a senior member of IEEE and is the current chairman of IEEE Cleveland section.

9:45 to 10:10

“Challenge and solution for high performance IF-Over-PCI system,” presented by Frederic Pirot of *R-Interface*

Abstract: Many applications require today an “easy to use” way of acquiring “on the air” data. The problem in itself is a challenge: target bandwidth can address a range going from a few Hertz to several Megahertz, with different output sampling frequency targets. On top of that, a good acquisition system must be able to acquire several different portions of the spectrum at a time and transfer the data at high data rate for post treatment such as demodulation. This presentation introduces a solution proposed by R-Interface based on a multiple, configurabl
on a PC. Live demonstration will be done using an high performance data acquisition board from Innovative DSP.

About the Speaker: Frederic Pirot is a design and system Manager at R-Interface. He provides system study, FPGA implementation and drivers on different reception systems. Prior to join R-Interface in 2008, Frederic worked at NXP, on Broadcats and telecommunication system specifications, DSP firmware implementation and VHDL blocs design for TV reception ASICs. Frédéric has master in engineering and electronics and is graduated from French Engineer school INSA.

10:30 to 10:55 "Automatic Synthesis of Flexible Multiprocessor Systems from Parallel Programs," presented by Harold Ishebabi of *Spectrum Signal Processing by Vecima*

Abstract: Multiprocessor architectures on FPGAs can be customized so that the execution of specific computational intensive software implementations, such as signal processing, can be optimized for speed or area. The design of such customized architectures is very complex, consisting of steps such as architecture determination, task mapping, scheduling as well as low level FPGA synthesis, placement and routing. The large size of the design space and non-orthogonal design parameters necessitate design automation through high-level synthesis to facilitate rapid explorations and implementations. This presentation introduces a design flow and high-level synthesis methodology that addresses these design challenges. The presentation will also cover software configuration and automation of vendor-specific FPGA tools in the flow.

About the Speaker: Harold Ishebabi is an Application Engineer at Spectrum Signal Processing by Vecima. He provides technical support and application development for wireless systems, specializing in algorithm, firmware and FPGA development. His experience includes research on programmable ASICs, fine and coarse-grained FPGAs for software defined radios. Mr. Ishebabi received his combined Bachelors and Masters degree in Electrical Engineering from the University of Kaiserslautern, Germany. He is expecting to receive his PhD in Computer Engineering in October 2009 from the University of Potsdam, Germany, where he has been working as an external part-time student.

10:55 to 11:20 "An Open Source FPGA Infrastructure for Heterogeneous Component-Based Systems," by Jim Kulp of *Mercury Federal Systems* and Shep Siegel, of *Atomic Rules, LLC*

Abstract: SDR, and the SCA specification have proven the efficacy of component-based development (CBD) for embedded systems. The optimal mix of processing technologies required in such systems is changing constantly, with technologies like multi-core, graphics proces
in this mix. This presentation will describe a close-to-the-metal open source CBD framework that supports SDR and SCA (as well as other embedded applications), across the range of technologies, focusing on the ever-present FPGA's role in the technology mix. This framework is currently being applied across a range of applications from SDR/SATCOM to RCIED/SIGINT and Airborne exploitation and surveillance.

About the Speakers: Jim Kulp, Consulting Software Architect at Mercury Federal Systems, Inc., has for more than 20 years, designed/developed/architected embedded/realtime and component-based systems software, IP and related standards for various embedded markets
Systems' multi-processor operating systems and middleware for more than 10 years, he has focused on advanced technologies and architectures in various DARPA, SDR, and other DoD efforts that combined CBD, heterogeneous, and parallel computing.

Shep Siegel, CTO of Atomic Rules, LLC, has enjoyed more than 25 years of practice in system architecture, applied digital signal proce
His contribution to transform coding, the invention of the Adaptive Zonal Coder, is cited by nearly 100 image and video processing patents. While at Mercury Computer Systems, Shep contributed to the development of IP comprising FPGA-based multicomputer nodes, led the adoption of the Open Core Protocol and Bluespec SystemVerilog, and helped transform these technologies into customer value.

11:20 to 11:45 "Hosting High Assurance Cryptographic architectures in an FPGA," by John Andolina of *ViaSAT*

Abstract: A cornerstone of Software Defined Radio (SDR) technology is the adaptive nature of the architecture to enable communication systems to be configured for multiple waveforms, and to operate over multiple networks. Manufactures of "Secure" SDR based c
strict certificate requirements. Traditional ASIC based cryptographic solutions used in legacy radios are not adaptive, relatively easy to reverse engineer, and if the algorithm is compromised, the radio and its network are unsecured. FPGA based cryptographic architectures are more difficult to reverse engineer and provide a higher lever of adaptive behavior that supports key requirements for Secure SDR based platforms. This presentation will describe an FPGA based cryptographic architecture, along with various implementations of that architecture used in a wide range of reprogrammable platforms. A proven FPGA based cryptographic architecture will be shown to be ideal and low risk for a secure, adaptive Software Defined and Cognitive Radio platform.

About the Speaker: John Andolina is the Director of Programmable Logic within ViaSat's Network Systems Group, and has over 15 years of experience in FPGA-based design. Within ViaSat's Network Systems Group, John has lead the FPGA development of several cryptographic designs and was a key contributor to the first NSA certified type-1 FPGA-based high assurance design. In addition, John has co-authored several ViaSat patents on the topic of FPGA-based cryptography. Prior to working in cryptography, John worked in the area of high-speed DSP and communication system design and received his M.S.E.E, and B.S.E.E from Rensselaer Polytechnic Institute.

11:45 to 12:15 "Processors for Digital Signal Processing: A Changing Landscape" by Jeff Bier, President, *BDTI*

Abstract: For most of the past 25 years, designers of demanding, digital-signal-processing-centric systems have largely relied on ASICs and digital signal processors (DSPs) as their main processing engines. Lately, however, the landscape of processing engine options has been shifting radically. As single-core DSPs have reached the point of diminishing returns, established processor vendors and start-ups alike have been increasingly relying on multi-core architectures. But multi-core architectures bring significant challenges in the realm of
increasingly seeing use as DSP engines, but these technologies bring their own development challenges. And, as digital signal processing ap

are becoming an attractive option for some applications. In this presentation, Jeff Bier will present highlights of some of BDTI's recent and ongoing evaluations of tradeoffs and trends in processing engines for signal processing applications.

1:30 to 1:55 "Using MATLAB and Simulink for the Design and Early Verification of Wireless Systems," presented by John Irza of *the Mathworks*

Abstract: Modern wireless system design has become increasingly more challenging, owing to the wide range of standards that a single system
implement a variety of modulation schemes, coding and equalization methods, and control and adaption techniques.

In this presentation we will demonstrate the modeling and simulation of a wireless system which includes system level effects such RF nonlinearities. The need-for and advantages-of early verification of a design will be highlighted through the use of system simulations that include RF impairments, the effects of fixed-point implementation, and the utilization of legacy HDL code in a co-simulation environment. A methodology will be presented which uses DSP and/or FPGA hardware-in-the-loop as part of the early verification approach to design.

About the Speaker: John Irza is a Technical Marketing Manager for The MathWorks communications products. His areas of focus include Cognitive Radio and Software Defined Radio, WiMAX and LTE systems, radar and sonar signal processing, and electronic warfare systems. Prior to joining The MathWorks in 2007, he was with Bluefin Robotics where he was a systems engineer integrating acoustic an
member of the technical staff, specializing in sonar and GPS systems for manned and unmanned undersea vehicles.

1:55 to 2:20 "Architecturally Optimized IP and High Level Synthesis for Rapid Algorithm Implementation and Verification in FPGA and ASIC technologies," presented by Doug Johnson of *Synopsis*

Abstract: This presentation outlines a model-based high level synthesis (HLS) methodology that enables a single algorithm model to drive architecturally optimized implementation and verification across multiple FPGA and ASIC technologies. The heart of the flow is a user-extensible library of IP that abstracts architecture and technology-dependent implementation details allowing easy high level design and simulation, bu
the system and IP level. The result is a consistent entry point for waveform algorithm design that is portable with automatic optimization and verification for multiple targets.

About the Speaker: Doug Johnson is a Staff Applications Consultant and DSP Product Specialist with the Synplicity Business Group of Synopsys, Inc. He is responsible for application engineering and product support for Synopsys' high-level synthesis, FPGA and ASIC logic synthesis and system-level design capture software products. Mr. Johnson has more than 30 years of experience in communication design engineering, electronic design automation (EDA) tools, applications engineering, digital signal processing (DSP) design, intellectual property (IP) licensing and sales account management. He has a BSEE from the University of Illinois at Urbana-Champaign.

2:20 to 2:45 "Next-Generation FPGA Middleware - Minimizing Latency in Multi-Processing SCA-Compliant Platforms," presented by Steve Jennis of *PrismTech*

Abstract: The SCA specification allows for two approaches to SCA waveform component compliance on FPGA: an abstraction layer (sometimes referred to as Modem Hardware Abstraction Layer or MHAL) or CORBA (as on GPP and DSP). In first-generation SCA radios a custom MHAL was often used, but introduced significant latency into the radio, as well as a non-standard interface layer with all the associated support and maintenance issues. CORBA was not then an option as a hardware implementation of an ORB was not available.

However, a hardware ORB implementation (Integrated Circuit ORB or ICO) has now been developed by PrismTech and tested by Selex Communication. The results of this testing show significantly lower latency as well as a relatively small 'gate or logic element' footprint for ICO. This is not surprising given the much more efficient architecture of ICO versus MHALs. Of course ICO is also based on an accepted middleware Standard, as opposed to the proprietary nature of MHALs.

This presentation w
in the next phase of ICO development and standardization.

The ICO Joint Industry Project (ICO JIP) is already supported by Selex Communications, Altera, and PrismTech and is open to any other participants and observers interested in influence over, and early access to, ICO technology for next-generation SCA radio designs.

About the Speaker: Steve Jennis joined PrismTech when it was a 'start-up' after a 16 year career with Texas Instruments. Steve has been a key executive in growing PrismTech's annual revenues to over $15M per annum and he led its entry into SDR COTS software in 2006. Today PrismTech has personnel in seven countries and is a recognized technology leader in software platforms and tools for real-time, distr
Loughborough University in England. Steve and his family have lived in Texas for the past 12 years.

3:00 to 3:30 "MHAL for FPGA" presented by Don Stephens of the *JTRS JPEO*

Abstract: The original Software Communications Architecture (SCA) specification did not include special consideration for the unique capabilities of Field Programmable Gate Arrays (FPGAs) or Digital Signal Processors (DSPs). Generalized Application Program Interfaces (APIs) for the DSPs and FPGA were released as part of the Joint Tactical Radio System (JTRS) Infrastructure, but the Modem Hardware Abstraction Layer (MHAL) API was based upon a 'push' model that mimics CORBA interfaces. It is highly abstracted and readily implemented with serial communication paths between processing elements.

While very extensible and scalable, the MHAL does not exploit the full capabilities of today's FPGAs and DSPs. Abstraction has been achieved at a cost of increased hardware/CPU resources, latency, and data copying. Although it supports serial interfaces between proc . An MHAL revision is in process that retains the scalability and extensibility of the original interface, but offers size, weight and power (SWAP) improvements in addition to improved communication response and performance.

About the Speaker: Donald R. Stephens, PhD, JPEO JTRS – San Diego. Dr. Stephens is the Standards Manager. His team is responsible for the establishment and standardization of the JTRS infrastructure. They are responsible for the various standards defined by the JTRS program including the SCA, APIs, and other interfaces and standards. He has lengthy development experience with software radios; including the Digital Modular Radio (DMR), the Joint Tactical Terminal (JTT), and the Airborne Integrated Terminal Group (AITG). Don has professional experience with Raytheon E-Systems, McDonnell Douglas, Emerson Electric, and Scientific Atlanta. He has participated in all technology facets of software radio design such as RF, DSP, distributed computing, security, and networking.

3:30 to 4:00 "OCP Corporate Introduction" presented by Ian Mackintosh, President and Chairman of *Open Core Protocol International Partnership (OCP-IP)*

Abstract: This presentation will provide an overview of the Open Cores Protocol, and will show how OCP supports design reuse in FPGA based applications.

About the Speaker: Ian Macintosh is the Chairman and President of OCP-IP. Mr. Mackintosh is well known in the EDA and Semiconductor industries as an ASIC pioneer with a background in semiconductor design, software development and business management. Mr. Mackintosh, founder of OCP-IP, has been historically on the Boards of groups dedicated to SoC development and IP exchange through open standards and has also chaired working group activity developing Standards for and investigation in, IP Protection. Since 1980, he has held various senior management positions with National Semiconductor, VLSI Technology (now NXP), PMC-Sierra, Mentor Graphics and several start-up companies. He holds a Masters of Science from Southampton University, England.

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