Efficient 3-D Extraction of Interconnect Capacitance Considering Floating Metal Fills With Boundary Element Method

Wenjian Yu, *Member, IEEE*, Mengsheng Zhang, and Zeyi Wang, *Member, IEEE*

***Abstract*—Inserting dummy (area fill) metals is necessary to reduce the pattern-dependent variation of dielectric thickness in the chemical–mechanical polishing (CMP) process. Such floating dummy metals affect interconnect capacitance and, therefore, signal delay and crosstalk significantly. To take the floating dummies into account, an efficient method for three-dimensional (3-D) capacitance extraction based on boundary element method is proposed. By introducing a floating condition into the direct boundary integral equation (BIE) and adopting an efficient preconditioning technique, and the quasi-multiple medium (QMM) acceleration, the method achieves very high computational speed. For some typical structures of area fill, the presented algorithm has shown over 1000× speedup over the industry-standard Raphael while preserving high accuracy. Compared with the recently proposed PASCAL in the work of Park *et al.* (2000), the proposed method also has about ten times speedup. Since the dummies are not regarded as normal electrodes in capacitance extraction, the proposed method is much more efficient than the conventional method, especially in cases with a large number of floating dummies.**

***Index Terms*—Boundary-element method (BEM), design for manufacturability, dummy fill, interconnect capacitance extraction.**

I. Introduction

FOR current very-large-scale integration (VLSI) circuit, chemical–mechanical polishing (CMP) is a necessary manufacturing step by which the wafer is polished with a rotating pad and slurry to achieve the planarized surfaces [1], [2]. Because the dielectric thickness strongly depends on the pattern density of underlying metal layer, a widely used method for reducing the variation of dielectric thickness in the CMP process is to insert dummy metals (this procedure is also called "area fill") [1]–[4]. These dummies are situated between signal lines to increase the pattern density and, at the same time, influence the electrical characteristics of interconnects in different ways depending on whether they are grounded or on the floating state. In the application-specific integrated circuit (ASIC) design, the floating dummy fills are preferred due to the short design period and considerable area to be filled. Such floating dummy fills have a strong impact on interconnect capacitance and, therefore, signal delay and crosstalk [1]–[3].

Nowadays, the area fill synthesis considering the impact on circuit performance has become an important problem of the design for manufacturability (DFM) [4]. For the electrical characterization or optimization of design rules for the dummy fills, a huge number of simulations are required for the structures involving floating dummy fills. However, most of the available parasitic extraction tools do not have specific treatment for floating dummies. For the case with floating conductors, a conventional field solver (such as SYNOPSYS Raphael) treats them as normal electrodes and extracts the full capacitance matrix. Then, the capacitance matrix is reduced by considering that the total charge on each floating conductor is equal to zero [5]. Obviously, the cost of central processing unit (CPU) time for extracting the full capacitance matrix is prohibitive while including a lot of floating dummies.

On the other hand, three-dimensional (3-D) interconnect capacitance extraction with the boundary element method (BEM) has drawn much attention recently, because of its advantage of dimensionality reduction over the finite difference method and finite element method. Many fast algorithms based on BEM have been proposed, including the fast multipole approach [6], hierarchical approach [7], the precorrected fast Fourier transform (FFT) algorithm [8], and the quasi-multiple medium (QMM) method [9], [10]. Different from other kinds of BEM, the QMM-accelerated BEM employs the direct boundary integral equation (BIE) [13], which has the property of resulting in a sparse coefficient matrix for a multiregion problem. By exploiting this character to enlarge the matrix sparsity and efficient techniques of equation organization and solution, the QMM–BEM solver has shown ten times speedup and memory saving over the multipole-accelerated method (FastCap 2.0) [6], for 3-D capacitance extraction [10].

In this paper, the QMM-accelerated BEM is extended to efficiently handle the structure with floating dummy fills. An equation corresponding to the floating condition is added into the discretized BEM equations, for each floating conductor. Then, with a new preconditioning technique for iterative equation solution, the interconnect capacitances are directly obtained. Since the floating conductor is not considered as normal electrode and no redundant capacitance entries need to be solved and reduced, the proposed method is much more efficient than the conventional method, particularly in the case of a great number of dummy fills in modern ASIC design.

Manuscript received July 11, 2004; revised December 15, 2004. This work was supported in part by the China National Science Foundation under Grant 90407004 and in part by the National High Technology Research and Development Program of China under Grant 2004AA1Z1050. This paper was recommended by Associate Editor W. Schoenmaker.

The authors are with the Department of Computer Science and Technology, Tsinghua University, Beijing 100084, China (e-mail: yu-wj@tsinghua.edu.cn).

Digital Object Identifier 10.1109/TCAD.2005.853690

Some typical structures of area fill are calculated to demonstrate the efficiency of the proposed method. Compared with Raphael (RC3), which is the finite difference solver with advanced nonuniform meshing, the proposed method has a speedup ratio above several hundreds.

In [11] and [15], two algorithms of capacitance extraction were proposed with specific consideration of the floating dummy fills. The algorithm in [15] is based on a so-called fictitious domain method, which uses the Lagrange multiplier λ to consider the conductor boundary and replaces the complex shape domain of potential computation with a simple one. However, no other algorithm was compared with the algorithm based on fictitious domain method, and the computational results in [15] did not show high efficiency (it costs 1 h for a structure including 130 floatings). The basic idea of [11] is similar to the authors, but the algorithm (called PASCAL) is implemented based on the finite difference method. Further work on electrical characterization of metal fills using the PASCAL can be found in [12]. Since the authors are not able to obtain the PASCAL for direct comparison in the same computational environment, an indirect comparison is carried out based on the speedup ratios to Raphael. For similar structures, the proposed method finally shows about ten times speedup over PASCAL.

The remainder of this paper is organized as follows. In Section II, the QMM-based capacitance extraction for structure without floating conductors is briefly reviewed. Efficient techniques handling the structure with floating dummies are presented in Section III. Experimental results are reported in Section IV, and conclusions are drawn in Section V.

II. Three-Dimensional Capacitance Extraction With the QMM-Accelerated BEM

In direct BEM, the Laplace equation fulfilled by the electrical potential u in each homogenous dielectric region can be transformed into the following direct BIEs [9], [10], [13]

$$cu + \int_{\Gamma_i} q^* u \mathrm{d}\Gamma = \int_{\Gamma_i} u^* q \mathrm{d}\Gamma \qquad i = 1, \ldots, M \tag{1}$$

where c is a constant depending on the boundary geometry and Γ_i is the boundary of dielectric region i (assuming there are totally M regions). q is the normal electrical field intensity and $q = \partial u/\partial \boldsymbol{n}$ where $\boldsymbol{n}$ means the vector outward normal to boundary. For 3-D space, the fundamental solution u^* is $1/4\pi r$ and $q^* = \partial u^*/\partial \boldsymbol{n}$. Employing constant quadrilateral elements to make boundary discretization and evaluating the direct BIE at collocation points (one for each element), the discretized BIEs are obtained from (1) for each dielectric region. After evaluating two types of boundary integral, a set of linear equations with unknowns of u and q is obtained [9].

Moreover, u and q fulfill the compatibility equations along the interface of two adjacent dielectrics a and b

$$\begin{cases} \varepsilon_{\mathrm{a}} \frac{\partial u_{\mathrm{a}}}{\partial \boldsymbol{n}_{\mathrm{a}}} = -\varepsilon_{\mathrm{b}} \frac{\partial u_{\mathrm{b}}}{\partial \boldsymbol{n}_{\mathrm{b}}} \\ u_{\mathrm{a}} = u_{\mathrm{b}} \end{cases} \tag{2}$$

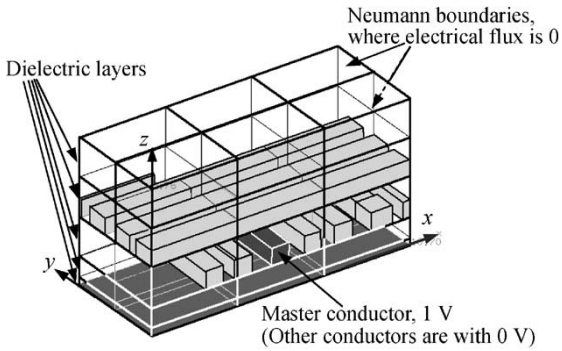

Fig. 1. Typical 3-D interconnect capacitor with five dielectric layers is cut into a 3×2 structure.

where ε_{a} and ε_{b} stand for the permittivities of dielectrics a and b, respectively. With (2) the u and q unknowns on the same interfacial element for both adjacent dielectric regions can be united, respectively. Therefore, the discretized BIEs for all dielectric regions can be put together. By substituting the boundary conditions (u is known on conductor surfaces as bias voltage, and q is supposed to be zero on the Neumann boundary as shown in Fig. 1), and preserving only the items of unknown variables to the left side of the equal sign, an overall linear system is obtained

$$\mathbf{A}\boldsymbol{x} = \boldsymbol{f} \tag{3}$$

where $\boldsymbol{x}$ is a vector comprising all discretized unknowns of u and q. Theoretically, any arrangement of the discretized BIEs in (3) is correct. However, without careful consideration, the population of the coefficient matrix $\mathbf{A}$ would be too chaotic to solve the equation efficiently. In [9], Yu *et al.* present an effective arrangement of the unknowns and collocation points, as well as the storage scheme for the resulting sparse matrix $\mathbf{A}$, which facilitates the matrix–vector multiplication in GMRES [14] equation solution for problem involving a large number of regions.

The above process can be regarded as the conventional direct BEM for a multiregion problem. A localization character is revealed by formula (1), where the variables in each BIE are within the same dielectric region. This character of direct BEM results in a blocked sparse coefficient matrix $\mathbf{A}$ for a multidielectric problem. For example, a typical capacitor with three dielectrics is shown in Fig. 2, and the corresponding sparse matrix $\mathbf{A}$ is shown in Fig. 3 (the effective equation arrangement is used). In the QMM method, every actual dielectric is decomposed into some fictitious medium blocks, whose permittivities are all the same as the original dielectric, to increase the sparsity of matrix $\mathbf{A}$. With the storage technique of sparse blocked matrix and efficient iterative equation solver such as the preconditioned GMRES algorithm, the computing time and memory usage for the original problem will be greatly reduced. In practice, each layer of an actual multilayered interconnect structure is decomposed into $m \times n$ fictitious medium blocks, perpendicular to the bottom substrate plane (see Fig. 1). In order to decrease the additional efforts brought by the QMM decomposition, the cutting planes are also dispersed along the x-axis or y-axis uniformly.

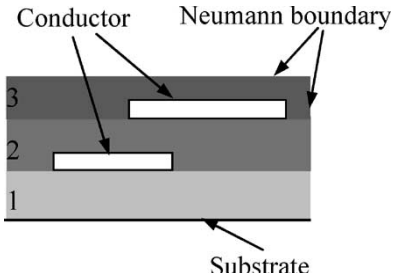

Fig. 2. Structure with three dielectrics (cross-sectional view).

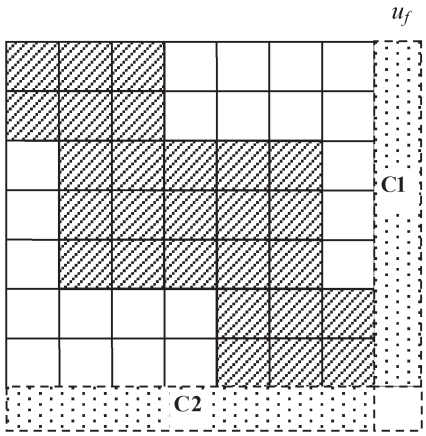

Fig. 3. Matrix population corresponding to the structure in Fig. 2 and the regions with dashed-line contour represent the added entries when considering the floating conductors.

In [10], an efficient approach to automatically determine the QMM cutting was proposed to maximize the sparsity of the overall coefficient matrix. Moreover, an efficient preconditioning technique was proposed for the GMRES solution, which resulted in about 30% less solution time than that using the Jacobi preconditioner. Finally, the enhanced QMM–BEM solver showed over ten times speedup and memory saving over the multipole approach with comparable accuracy [10].

III. Efficient Techniques Considering the Floating Dummies

In this section, first, the basic idea of the proposed method is given, which introduces the floating condition. The details of equation organization and preconditioning are then discussed. Finally, the proposed method is compared with the straightforward method for handling floating dummies.

A. Basic Idea

For a structure including N_c interconnect conductors, an approach of setting the jth conductor to 1 V and the rest to 0 V is usually used to determine the self and coupling capacitances of the jth conductor (it is also called master conductor). This procedure can be repeated N_c times to get the capacitance matrix, which includes all self and coupling capacitances among the interconnects. If there is no floating dummy in the structure, the potential u is known on all conductor surfaces. This boundary condition is utilized to form (3) in Section II. After solving (3), the self-capacitances and coupling capacitances can be evaluated by the integral of the normal electrical field intensity q on the conductor surfaces [6]–[10].

If some conductors in the simulated structure are changed to be floating (without setting known voltage), (3) cannot be solved because there are more unknowns (potential u on these floating conductors) than equations. So, the task at hand here is to supply additional equations about the floating dummies and make the enlarged system of linear equations solvable. The proposed method of capacitance extraction for the structure involving floating dummies includes six steps.

1) Set the jth interconnect conductor to 1 V and the rest interconnects to 0.
2) For each dielectric region, discretize its boundary (including dummy surface, since it is also a part of boundary) and formulate the discretized BIEs as in Section II.
3) Put the discretized BIEs for all regions together with (2), and substitute the known conditions on interconnect conductor surface and the Neumann boundary, as in Section II.
4) Supply some equations about the floating dummies so that the total number of equations is equal to the number of unknowns (including the additional u unknowns of dummies).
5) Solve the generated system of linear equations and get the charges on interconnect conductors that equal the capacitances.
6) Repeat steps 1)–5) with different voltage settings to get all capacitances among the interconnects.

Now, methods on how to supply the equations about the floating dummies are discussed. The following equation is used to calculate the total charge of a floating dummy

$$\int_{\Gamma_f} \sigma \mathrm{d}\Gamma = \int_{\Gamma_f} \varepsilon q \mathrm{d}\Gamma = \overline{Q}_f \tag{4}$$

where Γ_f is the surface of the dummy conductor, and σ is the surface charge density. ε is the permittivity of the dielectric surrounding surface Γ_f, and q is the normal electrical field intensity. Here, the charge $\overline{Q}_f$ is usually zero for each dummy as its initial electrical state. Since the dummy surface is discretized into elements, (4) is actually used as its discretized form, which involves discretized q unknowns on a dummy surface.

If there are N_f floating dummies, N_f new equations of (4) are derived, one for each dummy. On the other hand, as has been discussed, there are also N_f additional u unknowns of dummies, one for each dummy (because of the equipotential property). Hence, the extended equation system from (3) can be solved and the interconnect capacitances are then obtained.

B. Equation Organization and Preconditioning

As discussed above, more unknowns and equations are introduced for the case involving floating dummy fills. They are organized together with the initial discretized BEM equations

in (3) to form a new overall linear system. Putting (4) and the unknowns of potential on floating dummies at the end, the new linear system is derived with the form

$$\begin{bmatrix} \mathbf{A} & \mathbf{C1} \\ \mathbf{C2} & \mathbf{0} \end{bmatrix} \cdot \begin{bmatrix} \boldsymbol{x} \\ \boldsymbol{u}_f \end{bmatrix} = \begin{bmatrix} \boldsymbol{f} \\ \overline{\boldsymbol{q}} \end{bmatrix}, \quad \text{i.e., } \mathbf{A}'\boldsymbol{x}' = \boldsymbol{f}' \tag{5}$$

where $\mathbf{A}$, $\boldsymbol{x}$, and $\boldsymbol{f}$ are obtained from the linear system (3) where the floating character of dummies is not considered. $\boldsymbol{u}_f$ is the vector consisting of the unknown potential of dummies, and $\overline{\boldsymbol{q}}$ is made up of the right-hand side of (4) (actually a zero vector in the context of this paper). $\mathbf{C1}$ and $\mathbf{C2}$ are corresponding submatrices of coefficients. For the problem with three dielectrics in Fig. 2, if some conductors are changed to be floating, the modification of the overall coefficient matrix can be illustrated as the regions with dashed-line contour in Fig. 3.

Below, details of calculating the submatrices $\mathbf{C1}$ and $\mathbf{C2}$ with discretizing the direct boundary integrals (1) and (4) are given for a problem involving multiple dielectric regions and multiple floating dummies. $\mathbf{C1}$ corresponds to the coefficients of the new unknowns u_f and can be expressed as

$$(\mathbf{C1})_{ij} = \int\limits_{\partial\Omega_{f,j}^{(i)}} q_i^* \mathrm{d}\Gamma \tag{6}$$

where $q_{(i)}^*$ means the normal derivative of u^* in (1), which is related with the ith collocation point. $\partial\Omega_{f,j}^{(i)}$ represents the part of surface of the jth floating dummy, which is within the same dielectric region with the collocation point i. $\mathbf{C2}$ corresponds to the coefficients in (4), and can be expressed as

$$(\mathbf{C2})_{ij} = \begin{cases} \int_{\Gamma_j} \varepsilon \mathrm{d}\Gamma, & \text{when column } j \text{ corresponds} \\ & \text{to a } q \text{ unknown on dummy } i \\ 0, & \text{otherwise} \end{cases} \tag{7}$$

where Γ_j stands for the jth boundary element, and ε is the permittivity of the surrounding dielectric.

For capacitance extraction without floating dummies, a so-called extended Jacobi (EJ) preconditioner for GMRES algorithm was proposed in [10]. It is an approximation to $\mathbf{A}^{-1}$, and makes the convergence rate at least 30% faster than using the Jacobi preconditioner, while introducing little overhead [10]. However, since there is a zero diagonal block in $\mathbf{A}'$, the EJ preconditioner cannot be used here directly. Assume an EJ preconditioning matrix $\mathbf{P}$ is constructed for the original coefficient matrix $\mathbf{A}$, then the new preconditioner is constructed as follows:

$$\mathbf{P}' = \begin{bmatrix} \mathbf{P} & \mathbf{0} \\ \mathbf{0} & \mathbf{I} \end{bmatrix} \tag{8}$$

where $\mathbf{I}$ stands for the identity matrix. Since the dimension of $\mathbf{I}$ (equal to the number of dummies) is much smaller than the total number of discretized unknowns, $\mathbf{P}'$ still approximates $(\mathbf{A}')^{-1}$ to some extent. Therefore, the new preconditioner should also improve the rate of convergence for the GMRE equation solver. Numerical experiments verified this analysis.

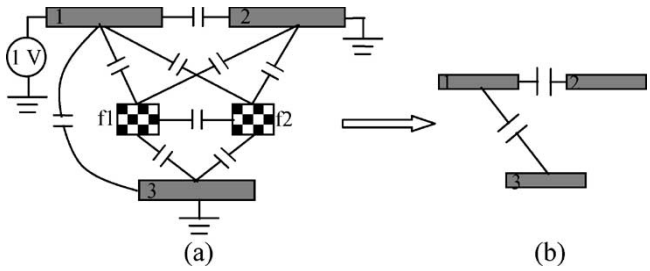

Fig. 4. Straightforward method of capacitance extraction for structure involving floating dummies. (a) Network of capacitances to be extracted. (b) Desired capacitance network after eliminating the floating nodes.

C. Comparison With the Straightforward Method

The straightforward method in conventional field solvers treats the floating dummies as normal electrodes, extracts the capacitances related with these dummies, and reduces them to get capacitances of interconnect. To illustrate this, a problem involving three interconnect conductors and two floating dummies is taken for example (see Fig. 4). If the coupling capacitances between conductor 1 and other interconnect conductors (2 and 3) ought to be calculated, i.e., conductor 1 is master conductor, all capacitances related with floating dummies [f1 and f2 in Fig. 4(a)] are first calculated. This invokes computing twice, with a floating dummy set to 1 V and the rest to 0 V. Then, conductor 1 is set to 1 V to calculate its capacitances. After that the capacitance network shown in Fig. 4(a) is obtained. Since f1 and f2 are floating, the network can be reduced to the one shown in Fig. 4(b) by eliminating the nodes of f1 and f2. Finally, the equivalent capacitance between conductor 1 and conductor 2 (or 3) is obtained, as if dummies do not exist. In fact, these equivalent capacitances are what the authors are concerned about.

For capacitance extraction of a structure involving N_c interconnect (signal) conductors and N_f floating dummies, the straightforward method is compared with the proposed method as follows.

1) To calculate the capacitances related with one master conductor (usually for the analysis of critical path), a 3-D field solver must be invoked for $(N_f + 1)$ times in the straightforward method, and then network reduction is performed to eliminate the floating nodes. In contrast, the 3-D field solver is invoked only once in the proposed method, although the degree of the linear system to be solved increases for N_f due to the additional unknowns of dummy potential. Usually in the field solution, the number of discretized unknowns is much larger than N_f. So the increased computational expense of the proposed method in the once field solution is very little. Ignoring both the increased expense of the proposed method and the time of network reduction in straightforward method, the speedup of the proposed method can be expected to be $(N_f + 1)$ for capacitance extraction with one master conductor.

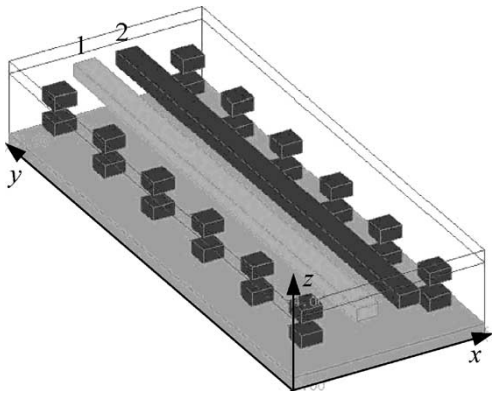

Fig. 5. Two conductor lines surrounded with 24 square floating dummies located at two layers.

2) To calculate the whole capacitance matrix of the interconnects, the 3-D field solver needs to be invoked for $(N_f + N_c)$ times in the straightforward method, while in the proposed method only N_c times are needed. Similarly, the proposed method has about $(N_c + N_f)/N_c$ times speedup over the straightforward one when extracting the whole capacitance matrix. This is also remarkable since N_f is usually much larger than N_c.

Therefore, for both the one-master extraction and the whole-matrix extraction, the proposed method has large speedup over the straightforward one. When there are a lot of dummies (N_f or N_f/N_c is large), the proposed method is particularly efficient compared with the straightforward method.

IV. Numerical Results

The proposed algorithm has been implemented in QBEM [10], a software prototype for 3-D capacitance extraction using the QMM-accelerated BEM. Some typical structures of floating dummy fills have been calculated to verify the efficiency of the proposed algorithm. All experiments are run on a Sun Ultra V880 with frequency of 750 MHz.

Three examples are shown in Figs. 5–7, respectively. The first one involves two parallel conductor lines surrounded with 24 square floating dummies located at two layers. The size of each conductor lines is $1 \times 23 \times 0.6$; the size of each dummy metal is $1 \times 1 \times 0.6$, and they all are within a window of size $9 \times 23 \times 4$, above the grounded substrate. The second one is a typical structure of floating dummy fills, which are arranged as a dot array in the oblique alignment and is often adopted for minimizing changes in the coupling capacitances and maximizing the uniformity of the pattern density [2], [11]. The size of each parallel conductor line is $6 \times 0.5 \times 0.5$; the size of each dummy metal is $0.5 \times 0.5 \times 0.5$, and they are all within a window of size $6 \times 9 \times 1.5$. In example 3 (Fig. 7), the dummy insertion rule is similar to that in the second example (Fig. 6), as dot array in the oblique alignment. Different from example 2, the conductor lines and dummies are located at two layers and the former constructs a 1×2 crossover. In this example, two conductor lines in the same layer are of size $6.5 \times 0.5 \times 0.5$, while the third one is of $0.5 \times 6.25 \times 0.5$. The size of each dummy is $0.5 \times 0.5 \times 0.5$, and all are within a window of size $6.5 \times 6.25 \times 2.5$. All length parameters above are in micrometer. The relative permittivities of layers in the same case are different, with values 1.9, 2.9, and 3.9.

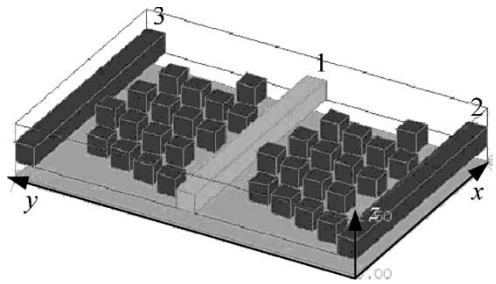

Fig. 6. Three conductor lines and 34 floating dummies of the dot-array type.

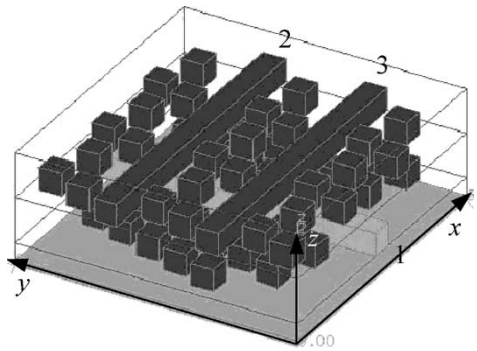

Fig. 7. Three conductor lines and 53 floating dummies of the dot-array type located at two layers.

In each of the three structures, conductor 1 is set to be a master (see Figs. 5–7), and its self-capacitance and coupling capacitances with other conductors are computed using Raphael and the proposed method. In the computation with Raphael, the dummy-related capacitances are calculated by setting each dummy as master conductor one after another, and the wanted capacitances are outputted after performing circuit reduction [5]. In the computations with the proposed method, 2×1, 1×3, and 4×2 QMM cutting are applied, respectively, for the three structures to achieve high speed. The capacitance results and other detailed data for these three examples are listed in Table I.

In Table I, it can be seen that the errors of capacitances computed with the proposed method are all within 3% (using Raphael's result as criterion), while the speedup ratio to Raphael ranges from 300 to several thousands. The proposed method uses less than one-tenth of the memory used by Raphael. It should also be pointed out that the electrical potential of dummy metal is also calculated, and it is very close to Raphael's result as well (with discrepancy within 5%). The number of dummies and number of unknowns in the proposed method are also listed in Table I, noting that the latter is larger than the element number because each interfacial element has two unknowns. From these data, it can be seen that the dummy number is much larger than the number of signal conductors, while the number of discretized unknowns is much larger than the number of dummies. They support some assumption for analysis in Section III.

TABLE I
COMPARISON OF COMPUTATIONAL RESULTS WITH OUR METHOD AND RAPHAEL (CAPACITANCE IN 10^{-18} F)

		Dummy_N	C_{11}	C_{12}	C_{13}	Ele_N	Var_N	Iter	Time (second)	Memory (megabyte)	Speed-Up
First Example	Proposed Method	24	2446	-1091	--	654	792	37	1.1	1.7	299
	Raphael		2470	-1088	--	$85\times10^{3*}$		--	328.4	18	--
Second Example	Proposed Method	34	766.1	-11.4	-10.4	1006	1172	55	1.9	2.7	1330
	Raphael		753.2	-11.5	-11.5	$281\times10^{3*}$		--	2527	54	--
Third Example	Proposed Method	53	732.1	-161.1	-141.5	1789	2501	52	3.0	5.9	2311
	Raphael		741.6	-163.0	-161.4	$385\times10^{3*}$		--	6932	72	--

Dummy_N means the number of dummies.
Ele_N means the number of elements in our method.
Var_N means the number of unknowns.
Iter means the number of iterative steps.
* Number of default grids generated by Raphael automatically.

TABLE II
COMPARISON OF COMPUTATIONAL TIME OF THE PROPOSED METHOD AND THE CONVENTIONAL METHOD FOR EXAMPLE 1

	Time for Extracting Capacitances Related With (second)			Total Time (second)	Speed-Up Ratio for One-Master Extraction	Speed-Up Ratio for Whole-Matrix Extraction
	Conductor 1	Conductor 2	24 Dummies			
Conventional Method	0.84	0.84	25.07	26.75	1	1
Proposed Method	1.13	1.13	--	2.26	**22.9**	**11.8**

To demonstrate the efficiency of the new preconditioner proposed in Section III-B, the problem is also solved without a preconditioner and with a modified Jacobi preconditioner. Experiment results show that without preconditioner the GMRES algorithm cannot converge within 300 steps for the last two problems and converges with 230 steps for the first problem. While using the modified Jacobi preconditioner, the iterative numbers for the three examples are 39, 62, and 62, respectively. Here, the modified Jacobi preconditioner is constructed also as (8). So, it is clear that the modified EJ preconditioner performs very well for the capacitance extraction involving floating dummies.

To demonstrate the advantage of our method over the conventional one, the whole capacitance matrix of example 1 is calculated using both methods. With the proposed method, QBEM ran twice, setting the two signal lines as master, respectively. With the conventional method, QBEM without the presented modification ran totally 26 times setting all conductors including dummies as master: one for each time. The details of computational time are listed in Table II. Without considering the time to eliminate the floating nodes, the speedup ratio of the proposed method is found to be 22.9 and 11.8, for single-master extraction and whole-matrix extraction, respectively. This is consistent with the theoretic analysis in Section III-C, which expects the speedup ratio to be 25 and 13. Because no more source of error is induced by the proposed method, it has the same accuracy with the conventional one.

In [11], a fast method to extract interconnect capacitance considering the floating dummy fills was implemented as software PASCAL, whose performance was also compared with Raphael. They used several cases of dummies located as dot arrays in the oblique alignment (similar to those in Fig. 6 and Fig. 7) to make a comparison, which showed that PASCAL has a speedup ratio varying from 11 to 290 (see [11, Table 2]) as the number of dummy metals increases. Since the PASCAL for direct comparison in the same computational environment cannot be obtained, only a relative comparison is carried out based on the information provided by [11]. Fig. 8 shows the speedup ratios of two methods to Raphael for similar structures involving oblique alignment of dot dummies. From this, it can be expected that the method in this paper is about ten times as fast as the PASCAL.

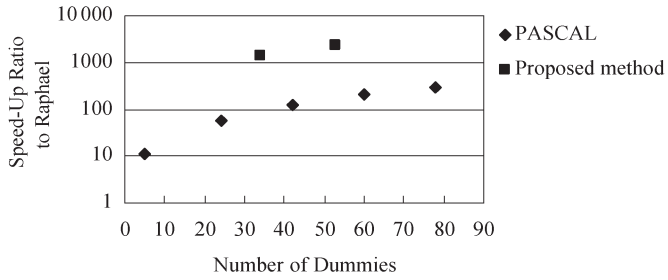

Fig. 8. Speedup ratio of PASCAL and the proposed method to Raphael for structures involving different numbers of dummies.

V. CONCLUSION

Based on the QMM-accelerated BEM [9], [10], an efficient method is proposed for the interconnect capacitance extraction involving dummy fills. By introducing the floating condition directly, only unknowns with quantity of dummy metals are added to the linear system corresponding to the same extraction problem except that the dummies are not floating. Since no redundant capacitances related with the dummies need to be solved and reduced, the proposed method is particularly efficient in the case of a great number of floating dummies. With the quasi-multiple medium technology and efficient preconditioned GMRES solver, the proposed method finally shows several thousand times speedup to Raphael while preserving high accuracy, for typical filling structures. Besides, the proposed method also shows about ten times speedup to the fast PASCAL in [11] for similar structures.

REFERENCES

[1] B. S. Stine *et al.*, "Rapid characterization and modeling of pattern dependent variation in chemical–mechanical polishing," *IEEE Trans. Semicond. Manuf.*, vol. 11, no. 1, pp. 129–140, Feb. 1998.

[2] A. B. Kahng *et al.*, "Filling algorithm and analyses for layout density control," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 18, no. 4, pp. 445–462, Apr. 1999.

[3] B. E. Stine, D. S. Boning, J. E. Chung *et al.*, "The physical and electrical effects of metal-fill patterning practices for oxide chemical–mechanical polishing processes," *IEEE Trans. Electron. Devices*, vol. 45, no. 3, pp. 665–679, Mar. 1998.

[4] Y. Chen, A. B. Kahng, G. Robins *et al.*, "Area fill synthesis for uniform layout density," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 21, no. 10, pp. 1132–1147, Oct. 2002.

[5] *Raphael Reference Manual*, Synopsys, Inc., San Jose, CA, Sep. 2003.

[6] K. Nabors and J. K. White, "Multipole-accelerated capacitance extraction algorithms for 3-D structures with multiple dielectrics," *IEEE Trans. Circuits Syst.*, vol. 39, no. 11, pp. 946–954, Nov. 1992.

[7] W. Shi, J. Liu, N. Kakani *et al.*, "A fast hierarchical algorithm for three-dimensional capacitance extraction," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 21, no. 3, pp. 330–336, Mar. 2002.

[8] J. R. Phillips and J. K. White, "A precorrected-FFT method for electrostatic analysis of complicated 3-D structures," *IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst.*, vol. 16, no. 10, pp. 1059–1072, Oct. 1997.

[9] W. Yu, Z. Wang, and J. Gu, "Fast capacitance extraction of actual 3-D VLSI interconnects using quasi-multiple medium accelerated BEM," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 1, pp. 109–120, Jan. 2003.

[10] W. Yu and Z. Wang, "Enhanced QMM–BEM solver for three-dimensional multiple-dielectric capacitance extraction within the finite domain," *IEEE Trans. Microw. Theory Tech.*, vol. 52, no. 2, pp. 560–566, Feb. 2004.

[11] J.-K. Park, K.-H. Lee, J.-H. Lee *et al.*, "An exhaustive method for characterizing the interconnect capacitance considering the floating dummy-fills by employing an efficient field solving algorithm," in *Proc. Int. Conf. Simulation Semiconductor Processes Devices*, Seattle, WA, Sep. 2000, pp. 98–101.

[12] W.-S. Lee, K.-H. Lee, J.-K. Park *et al.*, "Investigation of the capacitance deviation due to metal-fills and the effective interconnect geometry modeling," in *Proc. IEEE Int. Symp. Quality Electronic Design*, San Jose, CA, Mar. 2003, pp. 373–376.

[13] C. A. Brebbia, *The Boundary Element Method for Engineers*. London, U.K.: Pentech, 1978.

[14] Y. Saad and M. H. Schultz, "GMRES: A generalized minimal residual algorithm for solving nonsymmetric linear systems," *SIAM J. Sci. Stat. Comput.*, vol. 7, no. 3, pp. 856–869, 1986.

[15] O. Cueto, F. Charlet, and A. Farcy, "An efficient algorithm for 3D interconnect capacitance extraction considering floating conductors," in *Proc. Int. Conf. Simulation Semiconductor Processes Devices*, Kobe, Japan, Sep. 2002, pp. 107–110.

Wenjian Yu (S'00–M'03) received the B.S. and Ph.D. degrees in computer science, both with highest honors, from Tsinghua University, Beijing, China, in 1999 and 2003, respectively.

Since August 2003, he has been a Research Assistant in the Department of Computer Science and Technology at Tsinghua University. His research interests include parasitic parameter extraction of interconnects in very-large-scale integration (VLSI) circuits, direct boundary-element analysis of electromagnetic field, and modeling and simulation of VLSI interconnects. He has authored more than 30 technical papers published refereed journals and conference proceedings.

Dr. Yu was a Technical Program Subcommittee member of the ACM/IEEE Asia South-Pacific Design Automation Conference in 2005. He received the Microsoft Fellowship Award in 2002 and the distinguished Ph.D. Award from Tsinghua University in 2003. He has served as a Reviewer for the IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS.

Mengsheng Zhang received the B.S. degree in computer science in 2004 from Tsinghua University, Beijing, China, where he is currently working toward the Masters degree.

His main research interests include interconnect parasitics extraction and substrate coupling analysis.

Zeyi Wang (M'94) received the B.S. degree in computational mathematics in 1965 from Xian Jiaotong University, Xian, China.

Since 1965, he has been with Tsinghua University, Beijing, China, where he is currently a Professor with the Department of Computer Science and Technology. From 1987 to 1988, he was a Visiting Scholar at Stanford University, Stanford, CA, working on three-dimensional (3-D) device simulation on a parallel computer. His main research interests are the applications and research of the numerical methods, including the parallel computations in the areas of very-large-scale integration computer-aided design (VLSI-CAD) such as circuit analysis, device simulation, and parasitic interconnect parameter extraction.