An evolved circuit, intrinsic in silicon, entwined with physics.

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Introduction

- “Intrinsic” Hardware Evolution
    - “Intrinsic” used to indicate that fitness is evaluated for real, not merely in a simulation
    - Specific hardware: Xilinx XC6216 FPGA (Field Programmable Gate Array)

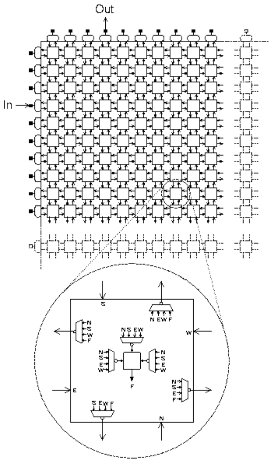
FPGA

- What is an FPGA?
  - Programmable hardware
  - Hardware can be designed in Verilog and VHDL
    - This experiment seemed to use neither

Xilinx XC6216

- Was still unreleased at time of experiment
- Array of 64 $\times$ 64 = 4,096 reconfigurable cells
  - Each cell connected to four neighbors
  - Each cell has a function unit that can perform any boolean function of two inputs
  - Output to each neighbor can be output from function unit or signal from another neighbor
  - Input and output occurs at edges of array
- Configuration held in on-chip memory
  - No configuration can damage device
    - Handy feature which allows genetic algorithm to do as it pleases unchecked

Diagram of Device



FPGA Setup

- Fixed input and output positions selected before beginning experiment
- Unused I/O points appeared as constant input
- Only used 10×10 corner of gate array
  - Other cells also simply produced a constant value
- Genotype encoding was string of 1,800 bits
  - Didn't give breakdown of bits

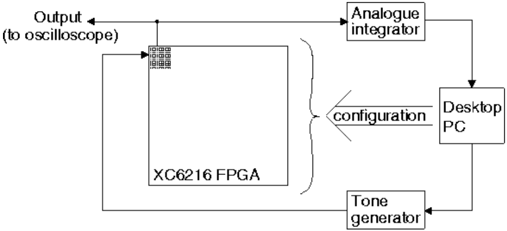
The Task

- Your task, should you choose to accept it: Discriminate between 1 kHz and 10 kHz input square waves by setting output to +5V for one and 0V for the other
  - Oh yeah, you get no clock or other external resources to help you time anything
  - And by 1 kHz and 10 kHz, we really mean 1.042 kHz and 10.416 kHz

GA Parameters

- Population size: 50
- Genotype encoding: strings of 1,800 bits
- Elitism of size 1
- Selection of other 49 offspring: linear rank-based
    - Such that fittest individual could expect twice as many offspring as the median individual
- Crossover probability: 0.7
- Mutation rate: Expected 2.7 mutations per genotype, so 0.0015 (0.15%)

Experimental Arrangement



Fitness Evaluation

- Tone generator generates 10 500ms tones: five of the 1 kHz variety, and five of the 10 kHz variety
  - The 10 tones are generated in a random order, with no gap in between
- Analog integrator reset to zero at beginning of each tone, and integrates output voltage over the tone's 500ms
- Analog integrator's value at end of tone is used in fitness function
- Note that fitness evaluation took over five seconds

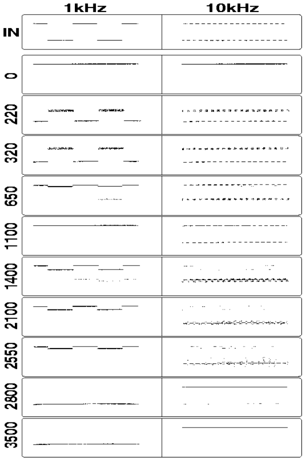
Fitness Function

$$\frac{1}{10}\left|\left(k_1 \sum_{t \in S_1} i_t\right) - \left(k_2 \sum_{t \in S_{10}} i_t\right)\right|$$

Where:

- i_t is analog integrator reading at end of test tone t, $1 \leq t \leq 10$
- S_1 is set of five 1 kHz test tones, S_{10} is set of five 10 kHz test tones
- $k_1 = \frac{1}{30{,}730.746}$ and $k_2 = \frac{1}{30{,}527.973}$
  - k_1 and k_2 determined experimentally such that circuit piping input directly to output receives zero fitness
    - Needed because otherwise that useless circuit becomes “an inescapable local optimum”

Oscilloscope Readings



Oscilloscope Interpretations

- Initial population: best individual produced a constant +5V
- Generation 220: best individual basically just copied input to output, but high part of wave had a high frequency component
- Generation 320: same as generation 220, but also occasional jumps to 0V when output should've been high
- Generation 650: much progress for 1 kHz input, with only occasional jumps to low voltage; highs and lows now match inputs
- Generation 1,100: 1 kHz works almost perfectly, 10 kHz still goofing around

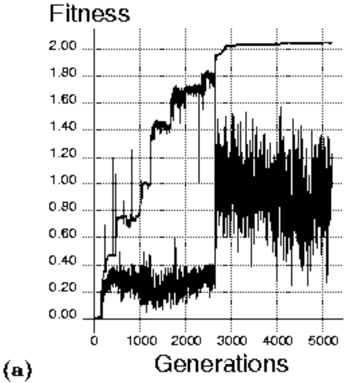
More Oscilloscope Interpretations

- Generation 1,400: 1 kHz not so perfect any more, but at least 10 kHz is mostly low now, while 1 kHz is still mostly high
- Generation 2,100: same general behavior but better
- Generation 2,550: still the same general behavior
- Generation 2,800: only defect is rapid glitching for 10 kHz input; high and low output have reversed
- Generation 3,500: almost perfect, except for infrequent unseen glitches

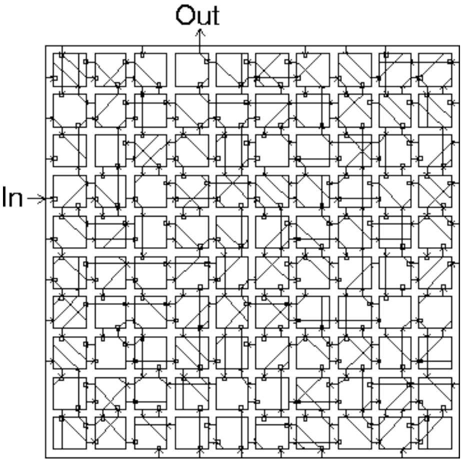
Last Unpictured Generations

- Generation 4,100: glitches from generation 3,500 eliminated (a.k.a., perfection)
- Generation 5,100: no observable change over last 1,000 generations

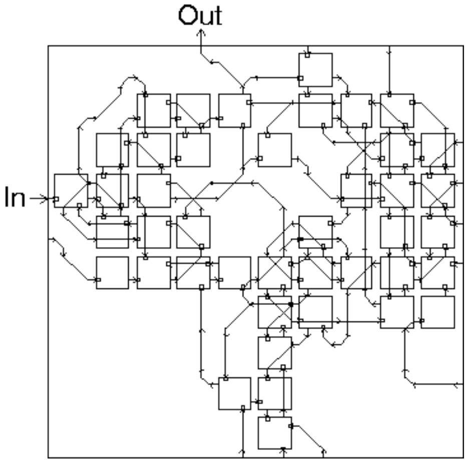
Fitness and Hamming Distance Graphs



Winning Circuit, Generation 5,000



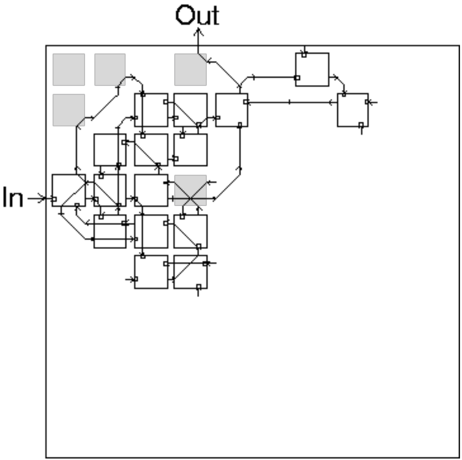
After Removing Elements with No Path to Output



Is This It?

- After removing all the cells and wires that have no possible path to the output, one might assume that what remains is the maximum necessary for circuit to work correctly
- One might be wrong
- Experiments were done where each cell had its function output clamped to a fixed value one by one, to see which cells were truly irrelevant
- *There turned out to be five cells which could not be clamped without degrading performance, although they had no possible connected path to the output*

Functional Part of Circuit



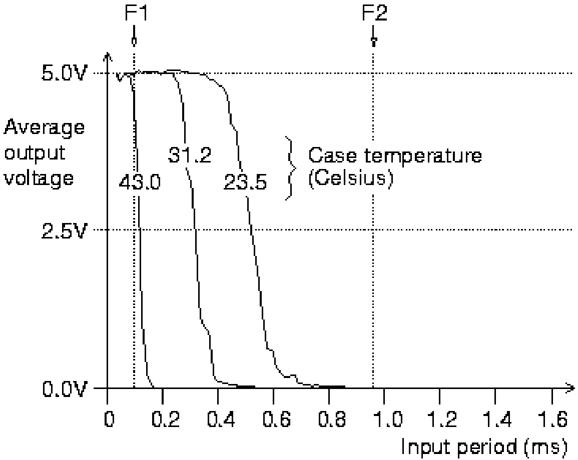
Explanation of Functional Part

- The gray boxes are the cells that had no path to the output, but which were still important to maintain performance
  - Cells in top left could be individually clamped, but clamping them all degraded performance noticeably
  - Lower-right gray cell single-handedly messes up performance severely if clamped
- Possible causes include interaction through the power supply and other electromagnetic interactions
- Small functional area means that this circuit should be tolerant of most hardware faults

Effect of Temperature

- During evolution, temperature was 31.2° C, ±5° C
- At that temperature, output is 0V for $\leq$ 1.6 kHz, and +5V for $\geq$ 4.5 kHz
- One might wonder how temperature affects these ranges of behavior

Performance at Different Temperatures



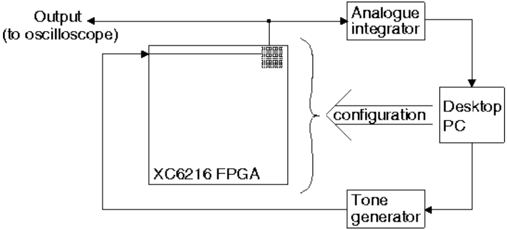
Interpretation

- Changing the temperature moves the performance curve left or right
- At 43°, 10 kHz is no longer on the flat plateau of stable +5V performance
- At 23.5°, 1 kHz is in a region that is still a little bumpy (or so we're told)
- These effects are because electronic components behave differently at different temperatures

Effect of Moving the Circuit

- One might ask oneself: “Self, given the subtle interactions between components that didn’t even have a path to the output, how sensitive is this circuit to this particular piece of hardware?”
- To find out, the population at generation 5,000 was moved to a completely different piece of the FPGA

Moving the Circuit



Results of Moving the Circuit

- The individual that performed best at the original location was about 7% worse at the new location
- However, a different individual was within 0.1% of perfection there
- After 100 generations of evolution at the new location, perfect performance had been attained again
- When this population was moved back to original position, the best individual at the other position was again degraded, but there was a different individual that performed perfectly

Questions

Got questions?