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A Robust Synchronizer

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Abstract

We describe a new latch circuit designed to give a high performance in low voltage synchronizer applications. By increasing the latch current only during metastability, we can more than maintain the value of the metastability time constant, t, without significantly increasing the power. Our circuit also reduces the variation of t with Vdd and temperature, so that it has a lower t at 50% Vdd than the conventional jamb latch has at 60% Vdd.

1. Introduction

An important effect of scaling is the increase in both dynamic and static power dissipation. Currently proposed solutions to this problem include dynamic lowering of the voltage in selected sub-systems when high performance is not required. Unfortunately, reduced power supplies usually disproportionately affect the performance of synchronizers since the synchronizer *t* depends on the small signal parameters in metastability rather than large signal switching times, and a 50% reduction in power supply voltage may result in over 100% increase in *t*. In this paper we present a circuit that is both faster than a conventional jamb latch synchronizer, and less sensitive to Vdd.

2. Jamb Latch

The Jamb latch is a simple circuit commonly used as a synchronizer because of its relatively good performance [1], and its basic configuration is shown in Figure 1. Here, the latch is reset by pulling node B to ground, and then set if data is high and clock is low, by pulling node A to ground. Metastability occurs if the overlap of data and clock is at a critical value that causes node A to be pulled down, and node B up to about the same voltage. By extensive use of SPICE simulation using parameters for a TSMC 0.18µ process, we optimised the transistor sizes for the Jamb Latch to give a low value for *t*. The results are shown in Table 1, and show a value for *t* at Vdd of 1.8v is 35.6ps.

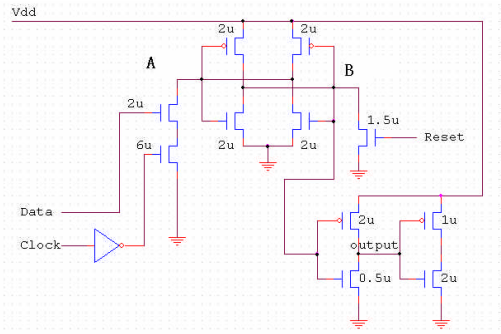

Figure 1 Jamb Latch

The minimum value of *t* is limited in this circuit by the capacitance of reset/set transistors, which cannot be further reduced in size, otherwise the circuit will not reliably set or reset. The optimum value of *t* is determined by both the capacitance and transconductance of the transistors when the circuit is in metastability. We found the best ratio between p-types and n-types is 1:1, a result also reported by others [1]. Table 1 also shows how *t* varies with Vdd and temperature for the Jamb Latch. It can be observed from Table 1 that *t* increases with Vdd decreasing and this reduction in speed becomes quite rapid where Vdd approaches the sum of thresholds of p and n-type transistors so that the value of τ is more than doubled at a Vdd of 0.9V, and more than an order of magnitude higher at 0.7V, -25 ^{o}C. For comparison we show the FO4 inverter delay in this technology that demonstrates τ is likely to track a processor clock period rather poorly, making design difficult. We also investigated the effect of increasing the width of all transistors by the same factor. In order to estimate the average energy used during metastability, we assume that the average metastability time is *t*. As the width increases, the total switching energy increases in proportion but τ only decreases slowly as transistor sizes increase, and reaches a limit at around 31ps.

Vdd(v)	τ(ps) at 27 °C	τ(ps) at -25 °C	FO4 at 27 °C	FO4 at -25 °C
1.8	35.6	29.5	91.6	78.6
1.7	36.8	30.5	94.2	80.9
1.6	38.3	31.8	97.3	83.6
1.5	40.1	33.3	100.9	86.8
1.4	42.4	35.4	105.3	90.6
1.3	45.4	38.0	110.5	95.3
1.2	49.4	41.8	117.0	101.1
1.1	55.2	47.3	125.2	108.6
1	63.8	56.2	136.0	118.5
0.9	78.5	72.8	150.7	132.1
0.8	106.8	114.6	171.9	151.2
0.7	252.8	522.2	203.3	182.7
0.6	754.7	1528.8	264.7	247.2

Table 1 Jamb latch τ vs Vdd

3. Improved Synchronizer

An improved synchronizer circuit that is much less sensitive to power supply variations is shown in Figure 2.

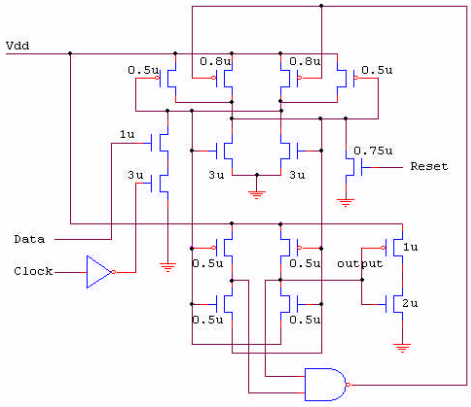

Figure 2 Improved synchronizer

Here the two 0.8µ p-type load transistors maintain sufficient current in the latch during metastability to keep the total transconductance high even at supply voltages less than the sum of thresholds of the p and n-type transistors. Two additional feedback p-types are added to the modified Jamb Latch in order to maintain the state of the latch when the main p-type loads are turned off. Because of these additional feedback p-types, the main p-types need only to be switched on during metastability, and the total power consumption is not excessive. A similar circuit has been described in [2], but few implementation details are given. In our implementation a metastability filter is used to produce the synchronizer output signals, which only go low if the two nodes have a significantly different voltage.

Vdd(v)	τ(ps) at 27 °C	τ(ps) at -25 °C
1.8	27.1	20.7
1.7	28.9	21.2
1.6	31.2	21.9
1.5	33.2	23.1
1.4	34.1	24.5
1.3	35.7	26.9
1.2	38.2	30.6
1.1	42.6	33.8
1	47.6	36.6
0.9	53.1	43.1
0.8	62.8	48.5
0.7	74.3	59.2
0.6	93.0	76.8

Table 2 Improved synchronizer τ vs Vdd

The outputs from the metastability filter are fed into a NAND gate to produce the control signal for the gates of two main p-types. In this circuit, the main p-types are off when the circuit is not switching, operating like a conventional jamb latch, but at lower power, when the circuit enters metastability the p-types are switched on to allow fast switching. The output is taken from the metastability filter, again to avoid any metastable levels being presented to following circuits. Now there is no need for the feedback p-types to be large, so set and reset can also be small. The optimum transistor sizes for the improved synchronizer are shown in Figure 2, and the resultant τ at Vdd of 1.8v is as low as 27.1ps because the main transconductance is provided by large n-type devices and because there are two additional p-types contributing to the gain. It also operates well at 0.6V Vdd and -25°C, because it does not rely on any series p and n-type transistors being both switched on by the same gate voltage. The relationship between τ and Vdd for the improved synchronizer is shown in Table 2. The switching energy for this circuit is 0.1783pj, compared with 0.1438pj for the conventional Jamb Latch. At the same time as maintaining a low value for *t*, the ratio between *t* and FO4 is much more constant at around 1:3 over a wide range of Vdd and temperature.

4 References

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